ISP1582

Hi-Speed Universal Serial Bus Peripheral Controller

Rev. 06 — 20 September 2007 Product data sheet

1. General description

The ISP1582 is a cost-optimized and feature-optimized Hi-Speed Universal Serial Bus (USB) Peripheral Controller. It fully complies with Ref. 1 “Universal Serial Bus Specification Rev. 2.0”, supporting data transfer at high-speed (480 Mbit/s) and full-speed (12 Mbit/s).

The ISP1582 provides high-speed USB communication capacity to systems based on microcontrollers or microprocessors. It communicates with a microcontroller or microprocessor of a system through a high-speed general-purpose parallel interface.

The ISP1582 supports automatic detection of Hi-Speed USB system operation. Original USB fall-back mode allows the device to remain operational under full-speed conditions. It is designed as a generic USB Peripheral Controller so that it can fit into all existing device classes, such as imaging class, mass storage devices, communication devices, printing devices and human interface devices.

The internal generic Direct Memory Access (DMA) block allows easy integration into data streaming applications.

The modular approach to implementing a USB Peripheral Controller allows the designer to select the optimum system microcontroller from the wide variety available. The ability to reuse existing architecture and firmware shortens the development time, eliminates risk and reduces cost. The result is fast and efficient development of the most cost-effective USB peripheral solution.

The ISP1582 also incorporates features such as SoftConnect, a reduced frequency crystal oscillator, and integrated termination resistors. These features allow significant cost savings in system design and easy implementation of advanced USB functionality into PC peripherals.

2. Features

- Complies fully with:
  - Ref. 1 “Universal Serial Bus Specification Rev. 2.0”
  - Most device class specifications
  - ACPI, OnNow and USB power management requirements
- Supports data transfer at high-speed (480 Mbit/s) and full-speed (12 Mbit/s)
- High performance USB Peripheral Controller with integrated Serial Interface Engine (SIE), Parallel Interface Engine (PIE), FIFO memory and data transceiver
- Automatic Hi-Speed USB mode detection and Original USB fall-back mode
- Supports sharing mode
- Supports V_{BUS} sensing

- Supports Generic DMA (GDMA) slave mode
- High-speed DMA interface
- Fully autonomous and multi-configuration DMA operation
- Seven IN endpoints, seven OUT endpoints, and a fixed control IN and OUT endpoint
- Integrated physical 8 kB of multi-configuration FIFO memory
- Endpoints with double buffering to increase throughput and ease real-time data transfer
- Bus-independent interface with most microcontrollers and microprocessors
- 12 MHz crystal oscillator with integrated PLL for low EMI
- Software-controlled connection to the USB bus (SoftConnect)
- Low-power consumption in operation and power-down modes; suitable for use in bus-powered USB devices
- Supports Session Request Protocol (SRP) that adheres to Ref. 2 “On-The-Go Supplement to the USB Specification Rev. 1.2”
- Internal power-on and low-voltage reset circuits; also supports software reset
- Operation over the extended USB bus voltage range (DP, DM and V_{BUS})
- 5 V tolerant I/O pads
- Operating temperature range from –40 °C to +85 °C
- Available in HVQFN56 halogen-free and lead-free package

3. Applications

- Personal digital assistant
- Digital video camera
- Digital still camera
- 3G mobile phone
- MP3 player
- Communication device, for example: router and modem
- Printer
- Scanner

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ISP1582BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-1

5. Block diagram

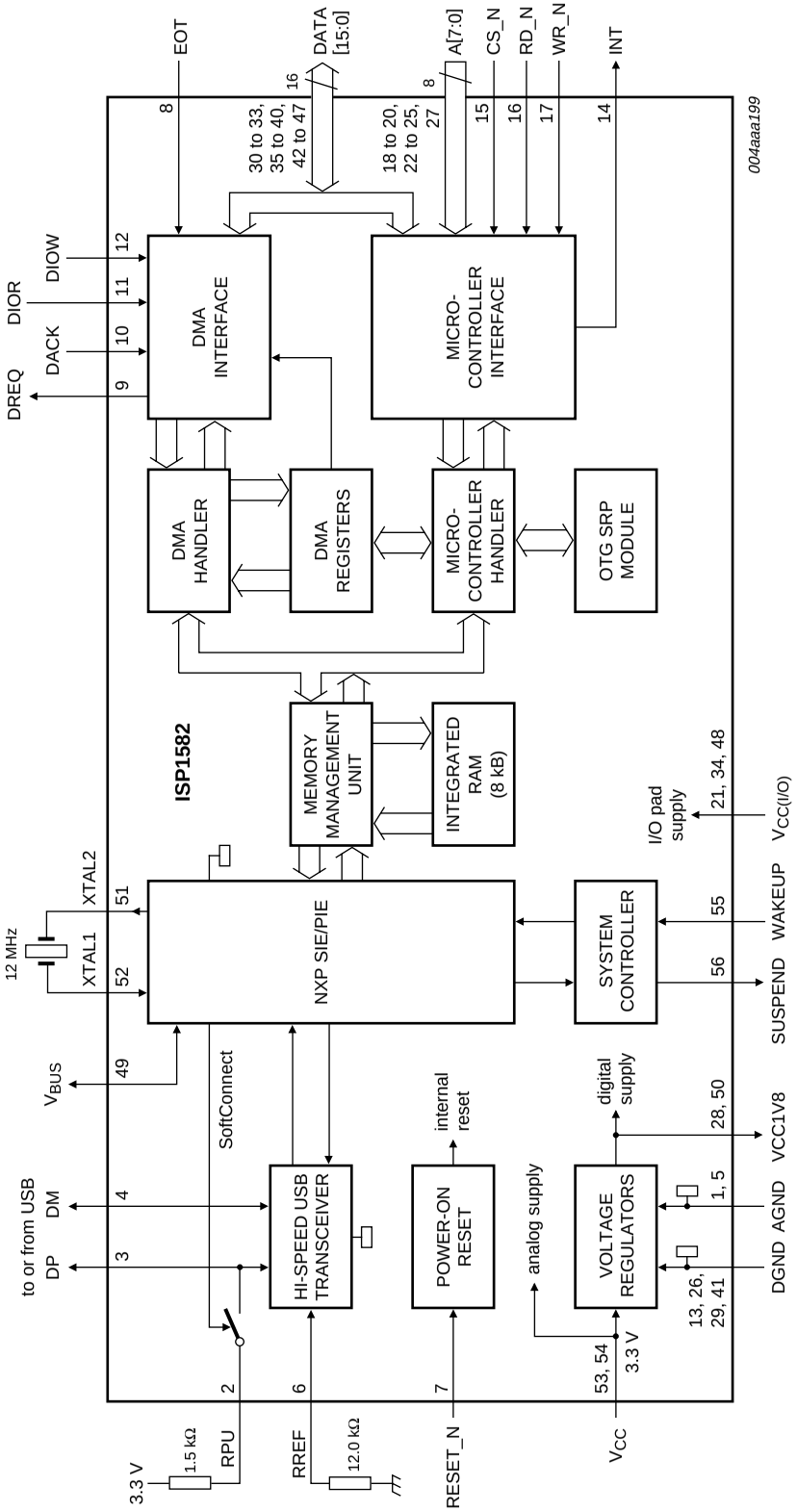


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

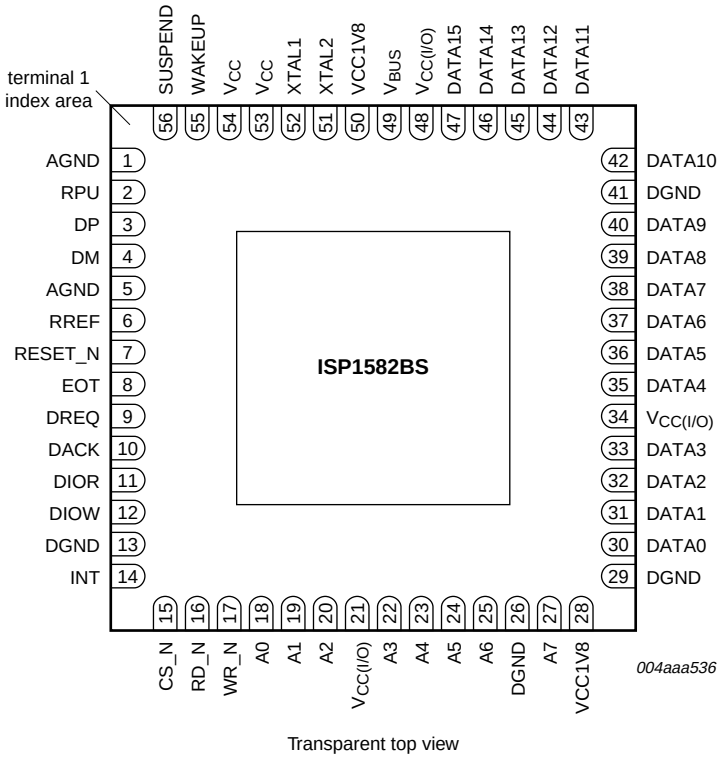


Fig 2. Pin configuration HVQFN56 (top view)

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Description
AGND	1	-	analog ground
RPU	2	A	pull-up resistor connection; connect to the external pull-up resistor for pin DP; must be connected to 3.3 V through a 1.5 kΩ resistor
DP	3	A	USB D+ line connection (analog)
DM	4	A	USB D– line connection (analog)
AGND	5	-	analog ground
RREF	6	A	external bias resistor connection; connect to the external bias resistor; must be connected to ground through a 12.0 kΩ ± 1 % resistor

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
RESET_N	7	I	reset input (500 µs); a LOW level produces an asynchronous reset; connect to V_{CC} for power-on reset (internal POR circuit) When the RESET_N pin is LOW, ensure that the WAKEUP pin does not goes from LOW to HIGH; otherwise the device will enter test mode. TTL; 5 V tolerant
EOT	8	I	end-of-transfer input (programmable polarity); when not in use, connect this pin to $V_{CC(I/O)}$ through a 10 kΩ resistor input pad; TTL; 5 V tolerant
DREQ	9	O	DMA request (programmable polarity) output; when not in use, connect this pin to ground through a 10 kΩ resistor; see Table 50 and Table 51 TTL; 4 ns slew-rate control
DACK	10	I	DMA acknowledge input (programmable polarity); when not in use, connect this pin to $V_{CC(I/O)}$ through a 10 kΩ resistor; see Table 50 and Table 51 TTL; 5 V tolerant
DIOR	11	I	DMA read strobe input (programmable polarity); when not in use, connect this pin to $V_{CC(I/O)}$ through a 10 kΩ resistor; see Table 50 and Table 51 TTL; 5 V tolerant
DIOW	12	I	DMA write strobe input (programmable polarity); when not in use, connect this pin to $V_{CC(I/O)}$ through a 10 kΩ resistor; see Table 50 and Table 51 TTL; 5 V tolerant
DGND	13	-	digital ground
INT	14	O	interrupt output; programmable polarity (active HIGH or LOW) and signaling (edge or level triggered) CMOS output; 8 mA drive
CS_N	15	I	chip select input input pad; TTL; 5 V tolerant
RD_N	16	I	read strobe input input pad; TTL; 5 V tolerant
WR_N	17	I	write strobe input input pad; TTL; 5 V tolerant
A0	18	I	bit 0 of the address bus input pad; TTL; 5 V tolerant
A1	19	I	bit 1 of the address bus input pad; TTL; 5 V tolerant
A2	20	I	bit 2 of the address bus input pad; TTL; 5 V tolerant
$V_{CC(I/O)}$[3]	21	-	supply voltage; used to supply voltage to the I/O pads; see Section 7.16
A3	22	I	bit 3 of the address bus input pad; TTL; 5 V tolerant

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
A4	23	I	bit 4 of the address bus input pad; TTL; 5 V tolerant
A5	24	I	bit 5 of the address bus input pad; TTL; 5 V tolerant
A6	25	I	bit 6 of the address bus input pad; TTL; 5 V tolerant
DGND	26	-	digital ground
A7	27	I	bit 7 of the address bus input pad; TTL; 5 V tolerant
VCC1V8[3]	28	-	regulator output voltage (1.8 V ± 0.15 V); tapped out voltage from the internal regulator; this regulated voltage cannot drive external devices; decouple this pin using a 0.1 µF capacitor; see Section 7.16
DGND	29	-	digital ground
DATA0	30	I/O	bit 0 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA1	31	I/O	bit 1 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA2	32	I/O	bit 2 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA3	33	I/O	bit 3 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
$V_{CC(I/O)}$[3]	34	-	supply voltage; used to supply voltage to the I/O pads; see Section 7.16
DATA4	35	I/O	bit 4 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA5	36	I/O	bit 5 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA6	37	I/O	bit 6 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA7	38	I/O	bit 7 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA8	39	I/O	bit 8 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA9	40	I/O	bit 9 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DGND	41	-	digital ground
DATA10	42	I/O	bit 10 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA11	43	I/O	bit 11 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA12	44	I/O	bit 12 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
DATA13	45	I/O	bit 13 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA14	46	I/O	bit 14 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
DATA15	47	I/O	bit 15 of bidirectional data bus bidirectional pad; 4 ns slew-rate control; TTL; 5 V tolerant
$V_{CC(I/O)}$[3]	48	-	supply voltage; used to supply voltage to the I/O pads; see Section 7.16
V_{BUS}	49	A	**USB bus power sensing input —** Used to detect whether the host is connected or not; connect a 1 µF electrolytic or tantalum capacitor and a 1 MΩ pull-down resistor to ground; see Section 7.14 **V_{BUS} pulsing output —** In OTG mode; connect a 1 µF electrolytic or tantalum capacitor and a 1 MΩ pull-down resistor to ground; see Section 7.14 5 V tolerant
VCC1V8[3]	50	-	voltage regulator output (1.8 V ± 0.15 V); tapped out voltage from the internal regulator; this regulated voltage cannot drive external devices; decouple this pin using 4.7 µF and 0.1 µF capacitors; see Section 7.16
XTAL2	51	O	crystal oscillator output (12 MHz); connect a fundamental parallel-resonant crystal; leave this pin open when using an external clock source on pin XTAL1; see Table 78
XTAL1	52	I	crystal oscillator input (12 MHz); connect a fundamental parallel-resonant crystal or an external clock source (leaving pin XTAL2 unconnected); see Table 78
V_{CC}[3]	53	-	supply voltage (3.3 V ± 0.3 V); this pin supplies the internal voltage regulator and the analog circuit; see Section 7.16
V_{CC}[3]	54	-	supply voltage (3.3 V ± 0.3 V); this pin supplies the internal voltage regulator and the analog circuit; see Section 7.16
WAKEUP	55	I	wake-up input; when this pin is at the HIGH level, the chip is prevented from getting into the suspend state and wake-up the chip when already in suspend mode; when not in use, connect this pin to ground through a 10 kΩ resistor When the RESET_N pin is LOW, ensure that the WAKEUP pin does not goes from LOW to HIGH; otherwise the device will enter test mode. input pad; TTL; 5 V tolerant
SUSPEND	56	O	suspend state indicator output; used as a power switch control output to power-off or power-on external devices when going into suspend mode or recovering from suspend mode CMOS output; 8 mA drive
GND	exposed die pad	-	ground supply; down bonded to the exposed die pad (heat sink); to be connected to DGND during PCB layout

[1] Symbol names ending with underscore N (for example, NAME_N) represent active LOW signals.

[2] All outputs and I/O pins can source 4 mA, unless otherwise specified.

[3] Add a decoupling capacitor (0.1 µF) to all the supply pins. For better EMI results, add a 0.01 µF capacitor in parallel to the 0.1 µF.

7. Functional description

The ISP1582 is a high-speed USB Peripheral Controller. It implements the Hi-Speed USB or the Original USB physical layer and the packet protocol layer. It concurrently maintains up to 16 USB endpoints (control IN, control OUT, and seven IN and seven OUT configurable) along with endpoint EP0 setup, which accesses the set-up buffer. The Ref. 1 "Universal Serial Bus Specification Rev. 2.0", Chapter 9 protocol handling is executed using the external firmware.

For high-bandwidth data transfer, the integrated DMA handler can be invoked to transfer data to or from external memory or devices. The DMA interface can be configured by writing to proper DMA registers (see Section 8.4).

The ISP1582 supports Hi-Speed USB and Original USB signaling. The USB signaling speed is automatically detected.

The ISP1582 has 8 kB of internal FIFO memory, which is shared among enabled USB endpoints, including control IN and control OUT endpoints, and set-up token buffer.

There are seven IN and seven OUT configurable endpoints, and two fixed control endpoints that are 64 bytes long. Any of the seven IN and seven OUT endpoints can be separately enabled or disabled. The endpoint type (interrupt, isochronous or bulk) and packet size of these endpoints can be individually configured, depending on the requirements of the application. Optional double buffering increases the data throughput of these data endpoints.

The ISP1582 requires 3.3 V power supply. It has 5 V tolerant I/O pads and an internal 1.8 V regulator to power the digital logic.

The ISP1582 operates on a 12 MHz crystal oscillator. An integrated 40 × PLL clock multiplier generates the internal sampling clock of 480 MHz.

7.1 DMA interface, DMA handler and DMA registers

The DMA block can be subdivided into two blocks: DMA handler and DMA interface.

The firmware writes to the DMA Command register to start a DMA transfer (see Table 43). The handler interfaces to the same FIFO (internal RAM) as used by the USB core. On receiving the DMA command, the DMA handler directs the data from the endpoint FIFO to the external DMA device or from the external DMA device to the endpoint FIFO.

The DMA interface configures the timing and the DMA handshake. Data can be transferred using either the DIOR and DIOW strobes or by the DACK and DREQ handshakes. DMA configurations are set up by writing to the DMA Configuration register (see Table 48 and Table 49).

Remark: The DMA endpoint buffer length must be a multiple of 4 bytes.

For details on DMA registers, see Section 8.4.

7.2 Hi-Speed USB transceiver

The analog transceiver directly interfaces to the USB cable through integrated termination resistors. The high-speed transceiver requires an external resistor (12.0 kΩ ± 1 %) between pin RREF and ground to ensure an accurate current mirror that generates the Hi-Speed USB current drive. A full-speed transceiver is integrated as well. This makes the ISP1582 compliant to Hi-Speed USB and Original USB, supporting both the high-speed and full-speed physical layers. After automatic speed detection, the NXP Serial Interface Engine (SIE) sets the transceiver to use either high-speed or full-speed signaling.

7.3 MMU and integrated RAM

The Memory Management Unit (MMU) manages the access to the integrated RAM that is shared by the USB, microcontroller handler and DMA handler. Data from the USB bus is stored in the integrated RAM, which is cleared only when the microcontroller has read the corresponding endpoint, or the DMA controller has written all data from the RAM of the corresponding endpoint to the DMA bus. The OUT endpoint buffer can also be forcibly cleared by setting bit CLBUF in the Control Function register. A total of 8 kB RAM is available for buffering.

7.4 Microcontroller interface and microcontroller handler

The microcontroller handler allows the external microcontroller or microprocessor to access the register set in the NXP SIE, as well as the DMA handler. The initialization of the DMA configuration is done through the microcontroller handler.

7.5 OTG SRP module

The OTG supplement defines a Session Request Protocol (SRP), which allows a B-device to request the A-device to turn on V_{BUS} and start a session. This protocol allows the A-device, which may be battery-powered, to conserve power by turning off V_{BUS} when there is no bus activity while still providing a means for the B-device to initiate bus activity.

Any A-device, including a PC or laptop, can respond to SRP. Any B-device, including a standard USB peripheral, can initiate SRP.

The ISP1582 is a device that can initiate SRP.

7.6 NXP high-speed transceiver

7.6.1 NXP Parallel Interface Engine (PIE)

In the High-Speed (HS) transceiver, the NXP PIE interface uses a 16-bit parallel bidirectional data interface. The functions of the HS module also include bit-stuffing or de-stuffing and Non-Return-to-Zero Inverted (NRZI) encoding or decoding logic.

7.6.2 Peripheral circuit

To maintain a constant current driver for HS transmit circuits and to bias other analog circuits, an internal band gap reference circuit and an RREF resistor form the reference current. This circuit requires an external precision resistor (12.0 kΩ ± 1 %) connected to the analog ground.

7.6.3 HS detection

The ISP1582 handles more than one electrical state, Full-Speed (FS) or High-Speed (HS), under the USB specification. When the USB cable is connected from the peripheral to the Host Controller, the ISP1582 defaults to the FS state, until it sees a bus reset from the Host Controller.

During the bus reset, the peripheral initiates an HS chirp to detect whether the Host Controller supports Hi-Speed USB or Original USB. If the HS handshake shows that there is an HS host connected, then the ISP1582 switches to the HS state.

In the HS state, the ISP1582 must observe the bus for periodic activity. If the bus remains inactive for 3 ms, the peripheral switches to the FS state to check for a Single-Ended Zero (SE0) condition on the USB bus. If an SE0 condition is detected for the designated time (100 µs to 875 µs; refer to Ref. 1 “Universal Serial Bus Specification Rev. 2.0”, Section 7.1.7.6), the ISP1582 switches to the HS chirp state to perform an HS detection handshake. Otherwise, the ISP1582 remains in the FS state, adhering to the bus-suspend specification.

7.6.4 Isolation

Ensure that the DP and DM lines are maintained in a clean state, without any residual voltage or glitches. Once the ISP1582 is reset and the clock is available, ensure that there are no erroneous pulses or glitches even of very small amplitude on the DP and DM lines.

Remark: If there are any erroneous unwanted pulses or glitches detected by the ISP1582 DP and DM lines, there is a possibility of the ISP1582 clocking this state into the internal core, causing unknown behaviors.

7.7 NXP Serial Interface Engine (SIE)

The NXP SIE implements the full USB protocol layer. It is completely hardwired for speed and needs no firmware intervention. The functions of this block include: synchronization pattern recognition, parallel or serial conversion, bit-stuffing or de-stuffing, CRC checking or generation, Packet IDentifier (PID) verification or generation, address recognition, handshake evaluation or generation.

7.8 SoftConnect

The USB connection is established by pulling pin DP (for full-speed devices) to HIGH through a 1.5 kΩ pull-up resistor. In the ISP1582, an external 1.5 kΩ pull-up resistor must be connected between pin RPU and 3.3 V. Pin RPU connects the pull-up resistor to pin DP, when bit SOFTCT in the Mode register is set (see Table 17 and Table 18). After a hardware reset, the pull-up resistor is disconnected by default (bit SOFTCT = 0). The USB bus reset does not change the value of bit SOFTCT.

When V_{BUS} is not present, the SOFTCT bit must be set to logic 0 to comply with the back-drive voltage.

7.9 Clear buffer

Use clear buffer when data needs to be discarded under the following conditions:

- IN endpoint: If the host aborts a read operation, the residual data in the IN endpoint buffer must be cleared using the CLBUF bit. See Table 31. For details on clearing the IN buffer, refer to Ref. 4 “ISP1582/83 and ISP1761 clearing an IN buffer (AN10045)”.
- OUT endpoint: If the host aborts a write operation, the residual data in the OUT endpoint buffer must be cleared using the CLBUF bit. See Table 31.

For example, to clear a double buffer data OUT endpoint 1, set the following registers in the firmware as:

1. Assign a value to the DMA Endpoint register. It can be any value other than the value assigned to the Endpoint Index register. In this example, do not assign 2h to the DMA Endpoint register. See remark in Section 8.3.1.
2. Assign Endpoint Index register = 2h
3. Assign Control Function register = 10h
4. Assign Endpoint Index register = 2h
5. Assign Control Function register = 10h

7.10 Reconfiguring endpoints

The ISP1582 endpoints have a limitation when implementing a composite device with at least two functionalities that require the support of alternate settings, for example, the video class and audio class devices. The ISP1582 endpoints cannot be reconfigured on the fly because it is implemented as a FIFO base. The internal RAM partition will be corrupted if there is a need to reconfigure endpoints on the fly because of alternate settings request, causing data corruption.

For details and work-around, refer to Ref. 3 “ISP1581/2/3 Frequently Asked Questions (AN10046)”.

7.11 System controller

The system controller implements the USB power-down capabilities of the ISP1582. Registers are protected against data corruption during wake-up following a resume (from the suspend state) by locking the write access, until an unlock code is written in the Unlock Device register (see Table 68 and Table 69).

7.12 Pins status

Table 3 illustrates the behavior of ISP1582 pins with $V_{CC(I/O)}$ and V_{CC} in various operating conditions.

Table 3. ISP1582 pin status

V_{CC}	$V_{CC(I/O)}$	State	Pin		
			Input	Output	I/O
0 V	0 V	dead[1]	unknown	unknown	unknown
0 V	V_{CC}	plug-out[2]	high-Z	unknown	high-Z

Table 3. ISP1582 pin status *…continued*

V_{CC}	$V_{CC(I/O)}$	State	Pin		
			Input	Output	I/O
0 V → 3.3 V	V_{CC}	plug-in[3]	high-Z	unknown	high-Z
3.3 V	V_{CC}	reset	state depends on how the pin is driven	output	high-Z
3.3 V	V_{CC}	after reset	state depends on how the pin is driven	output	state depends on how the pin is configured

[1] Dead: the USB cable is plugged out, and $V_{CC(I/O)}$ is not available.

[2] Plug-out: the USB cable is not present, but $V_{CC(I/O)}$ is available.

[3] Plug-in: the USB cable is being plugged in, and $V_{CC(I/O)}$ is available.

Table 4 illustrates the behavior of output pins with $V_{CC(I/O)}$ and V_{CC} in various operating conditions.

Table 4. ISP1582 output status

V_{CC}	$V_{CC(I/O)}$	State	INT	SUSPEND
0 V	0 V	dead[1]	X[2]	X[2]
0 V	V_{CC}	plug-out[3]	LOW	HIGH
0 V → 3.3 V	V_{CC}	plug-in[4]	LOW	HIGH
3.3 V	V_{CC}	reset	HIGH	LOW
3.3 V	V_{CC}	after reset	HIGH	LOW

[1] Dead: The USB cable is plugged-out and $V_{CC(I/O)}$ is not available.

[2] X: Don't care.

[3] Plug-out: The USB cable is not present but $V_{CC(I/O)}$ is available.

[4] Plug-in: The USB cable is being plugged-in and $V_{CC(I/O)}$ is available.

7.13 Interrupt

7.13.1 Interrupt output pin

The Interrupt Configuration register of the ISP1582 controls the behavior of the INT output pin. The polarity and signaling mode of pin INT can be programmed by setting bits INTPOL and INTLVL of the Interrupt Configuration register (R/W: 10h); see Table 21. Bit GLINTENA of the Mode register (R/W: 0Ch) is used to enable pin INT. Default settings after reset are active LOW and level mode. When pulse mode is selected, a pulse of 60 ns is generated when the OR-ed combination of all interrupt bits changes from logic 0 to logic 1.

Figure 3 shows the relationship between interrupt events and pin INT.

Each of the indicated USB and DMA events is logged in a status bit of the Interrupt register and the DMA Interrupt Reason register, respectively. Corresponding bits in the Interrupt Enable register and the DMA Interrupt Enable register determine whether an event will generate an interrupt.

Interrupts can be masked globally by means of bit GLINTENA of the Mode register; see Table 18.

Field CDBGMOD[1:0] of the Interrupt Configuration register controls the generation of INT signals for the control pipe. Field DDBGMODIN[1:0] of the Interrupt Configuration register controls the generation of INT signals for the IN pipe. Field DDBGMODOUT[1:0] of the Interrupt Configuration register controls the generation of INT signals for the OUT pipe; see Table 22.

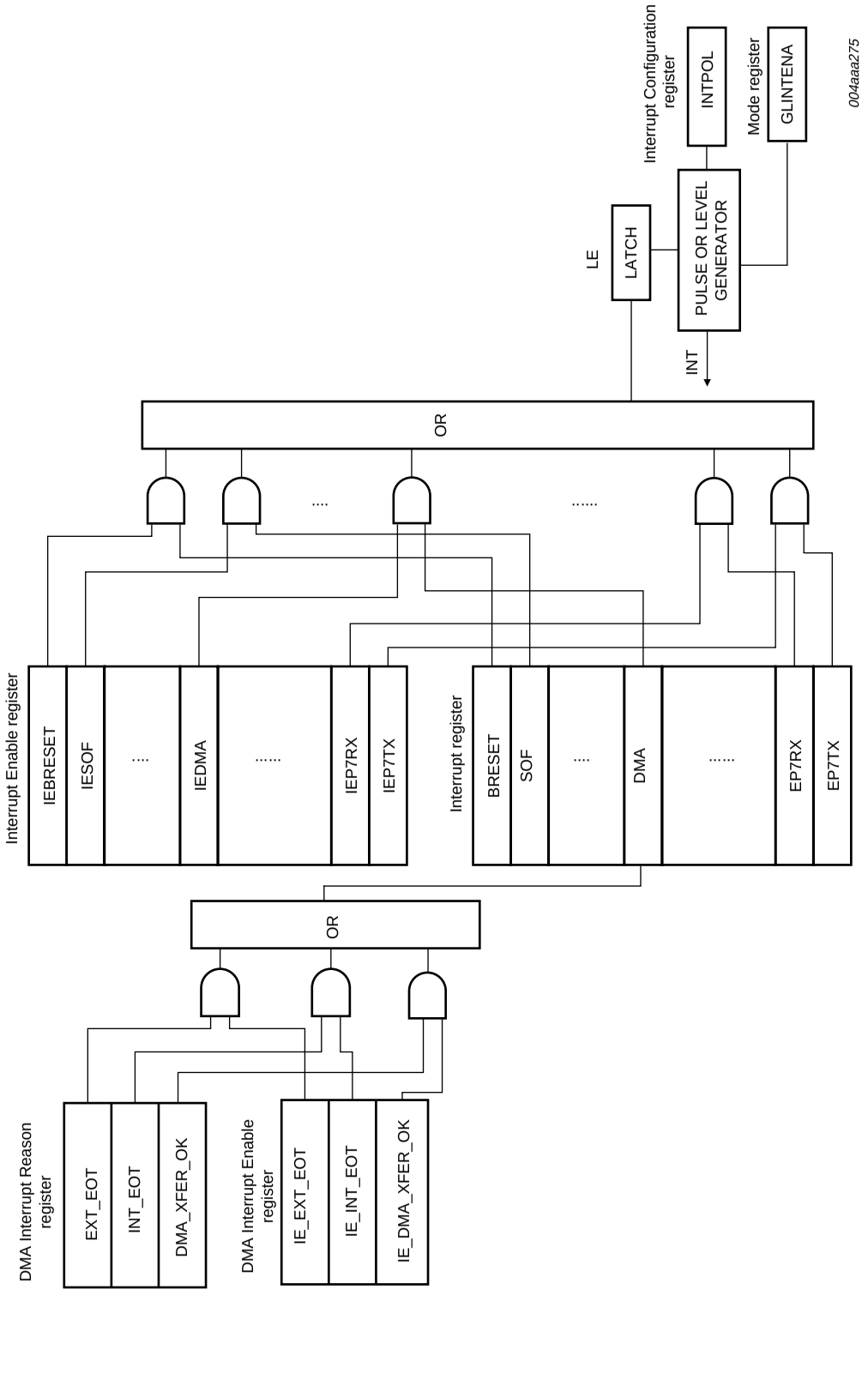


Fig 3. Interrupt logic

7.13.2 Interrupt control

Bit GLINTENA in the Mode register is a global interrupt enable or disable bit. The behavior of this bit is given in Figure 4.

The following illustrations are only applicable for level trigger.

Event A: When an interrupt event occurs (for example, SOF interrupt) with bit GLINTENA set to logic 0, an interrupt will not be generated at pin INT. It will, however, be registered in the corresponding Interrupt register bit.

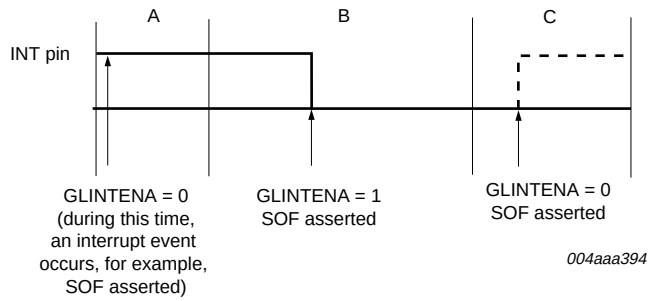
Event B: When bit GLINTENA is set to logic 1, pin INT is asserted because bit SOF in the Interrupt register is already set.

Event C: If the firmware sets bit GLINTENA to logic 0, pin INT will still be asserted. The bold line shows the desired behavior of pin INT.

De-assertion of pin INT can be achieved either by clearing all the bits in the Interrupt register or the DMA Interrupt Reason register, depending on the event.

Remark: When clearing an interrupt event, perform write to all the bytes of the register.

For more information on interrupt control, see Section 8.2.2, Section 8.2.5 and Section 8.5.1.



Pin INT: HIGH = de-assert; LOW = assert (individual interrupts are enabled).

Fig 4. Behavior of bit GLINTENA

7.14 V_{BUS} sensing

The V_{BUS} pin is one of the ways to wake up the clock when the ISP1582 is suspended with bit CLKAON set to logic 0 (clock off option).

To detect whether the host is connected or not, that is V_{BUS} sensing, a 1 MΩ resistor and a 1 µF electrolytic or tantalum capacitor must be added to damp the overshoot on plug-in.

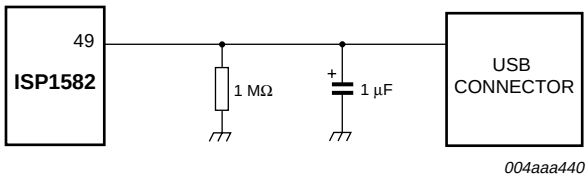


Fig 5. Resistor and electrolytic or tantalum capacitor needed for V_{BUS} sensing

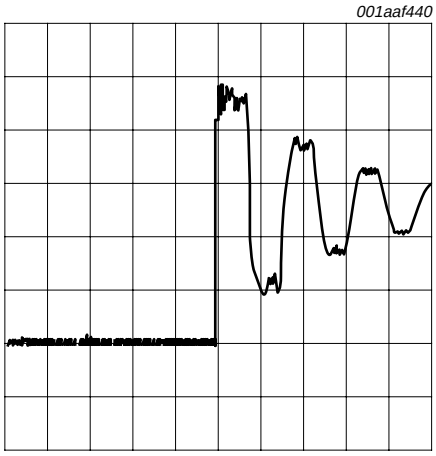


Fig 6. Oscilloscope reading: no resistor and capacitor in the network

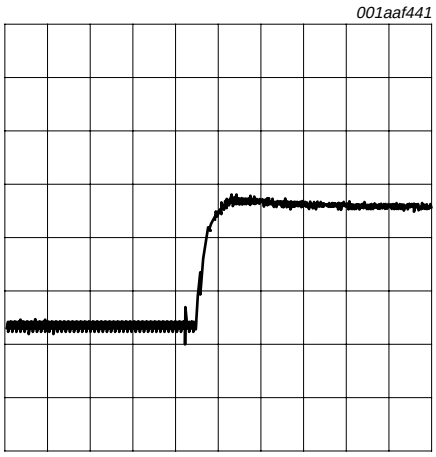


Fig 7. Oscilloscope reading: with resistor and capacitor in the network

7.15 Power-on reset

The ISP1582 requires a minimum pulse width of 500 µs.

The RESET_N pin can either be connected to V_{CC} (using the internal POR circuit) or externally controlled (by the microcontroller, ASIC, and so on). When V_{CC} is directly connected to the RESET_N pin, the internal pulse width t_{PORP} will typically be 200 ns.

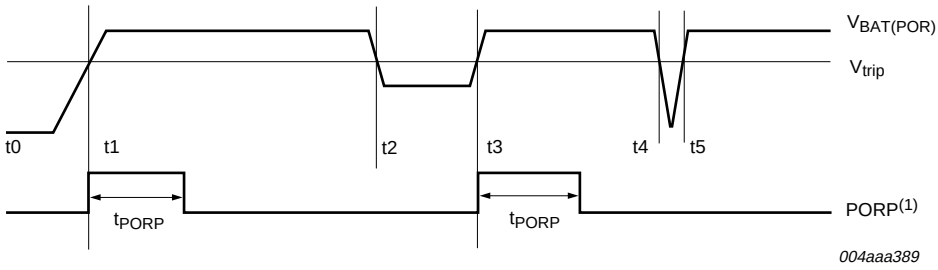
The power-on reset function can be explained by viewing the dips at t2 to t3 and t4 to t5 on the $V_{CC(POR)}$ curve (Figure 8).

t0 — The internal POR starts with a HIGH level.

t1 — The detector will see the passing of the trip level and a delay element will add another t_{PORP} before it drops to LOW.

t2-t3 — The internal POR pulse will be generated whenever $V_{CC(POR)}$ drops below V_{trip} for more than 11 µs.

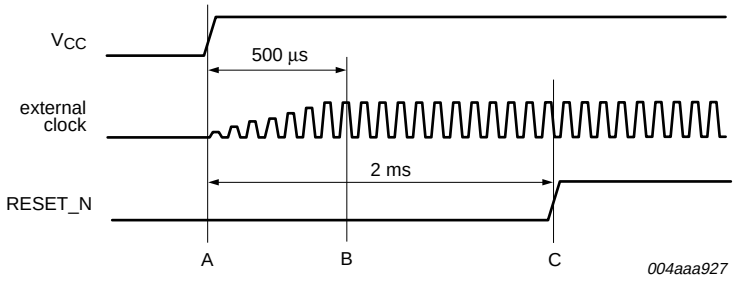
t4-t5 — The dip is too short (< 11 µs) and the internal POR pulse will not react and will remain LOW.



(1) PORP = Power-On Reset Pulse.

Fig 8. POR timing

Figure 9 shows the availability of the clock with respect to the external POR.



Power on V_{CC} at A.

Stable external clock is to be available at B.

The ISP1582 is operational at C.

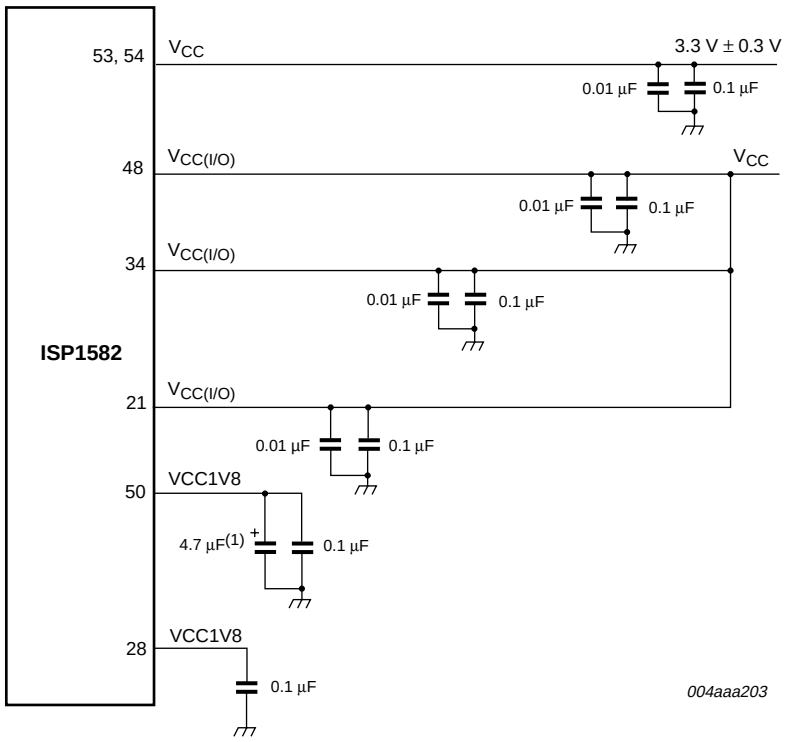
Fig 9. Clock with respect to the external POR

7.16 Power supply

The ISP1582 can be powered by 3.3 V ± 0.3 V, and 3.3 V at the interface. For connection details, see Figure 10.

If the ISP1582 is powered by V_{CC} = 3.3 V, an integrated 3.3 V-to-1.8 V voltage regulator provides a 1.8 V supply voltage for the internal logic.

In sharing mode (that is, when V_{CC} is not present and $V_{CC(I/O)}$ is present), all I/O pins are input type, the interrupt pin is connected to ground, and the suspend pin is connected to $V_{CC(I/O)}$. See Table 3.



(1) At the V_{CC} input (3.3 V) to the USB controller, if the ripple voltage is less than 20 mV, then 4.7 µF standard electrolytic or tantalum capacitors (tested ESR up to 10 Ω) should be OK at the VCC1V8 output. If the ripple voltage at the input is higher than 20 mV, then use 4.7 µF LOW ESR capacitors (ESR from 0.2 Ω to 2 Ω) at the VCC1V8 output. This is to improve the high-speed signal quality at the USB side.

Fig 10. ISP1582 with 3.3 V supply

Table 5 shows power modes in which the ISP1582 can be operated.

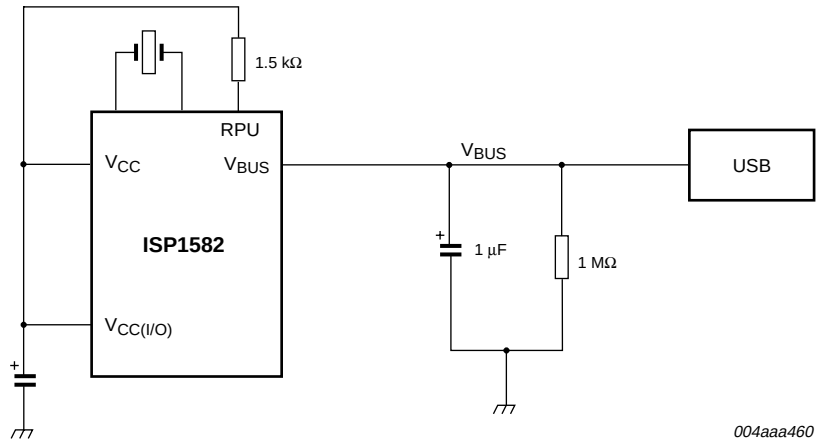
Table 5. Power modes

V_{CC}	$V_{CC(I/O)}$	Power mode
V_{BUS}[1]	V_{BUS}[2]	bus-powered
System-powered	system-powered	self-powered

[1] The power supply to the IC (V_{CC}) is 3.3 V. Therefore, if the application is bus-powered, a 3.3 V regulator needs to be used.

[2] $V_{CC(I/O)} = V_{CC}$. If the application is bus-powered, a voltage regulator must be used.

7.16.1 Self-powered mode



$V_{CC(I/O)}$ and V_{CC} are system powered.

Fig 11. Self-powered mode

In self-powered mode, V_{CC} and $V_{CC(I/O)}$ are supplied by the system. See Figure 11.

Table 6. Operation truth table for SoftConnect

ISP1582 operation	Power supply				Bit SOFTCT in Mode register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Normal bus operation	3.3 V	3.3 V	3.3 V	5 V	enabled
No pull-up on DP	3.3 V	3.3 V	3.3 V	0 V[1]	disabled

[1] When the USB cable is removed, SoftConnect is disabled.

Table 7. Operation truth table for clock off during suspend

ISP1582 operation	Power supply				Clock off during suspend
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Clock will wake up: After resume and After a bus reset	3.3 V	3.3 V	3.3 V	5 V	enabled
Clock will wake up: After detecting the presence of V_{BUS}	3.3 V	3.3 V	3.3 V	0 V → 5 V	enabled

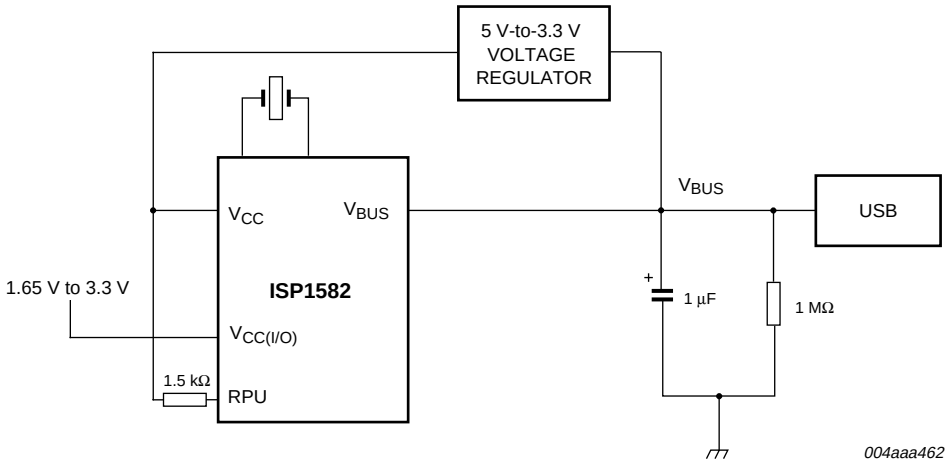
Table 8. Operation truth table for back voltage compliance

ISP1582 operation	Power supply				Bit SOFTCT in Mode register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Back voltage is not measured in this mode	3.3 V	3.3 V	3.3 V	5 V	enabled
Back voltage is not an issue because pull up on DP will not be present when V_{BUS} is not present	3.3 V	3.3 V	3.3 V	0 V	disabled

Table 9. Operation truth table for OTG

ISP1582 operation	Power supply				OTG register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
SRP is not applicable	3.3 V	3.3 V	3.3 V	5 V	not applicable
SRP is possible	3.3 V	3.3 V	3.3 V	0 V	operational

7.16.2 Bus-powered mode



$V_{CC(I/O)}$ is powered by V_{BUS}.

Fig 12. Bus-powered mode

In bus-powered mode (see Figure 12), V_{CC} and $V_{CC(I/O)}$ are supplied by the output of the 5 V-to-3.3 V voltage regulator. The input to the regulator is from V_{BUS}. On plugging the USB cable, the ISP1582 goes through the power-on reset cycle. In this mode, OTG is disabled.

Table 10. Operation truth table for SoftConnect

ISP1582 operation	Power supply				Bit SOFTCT in Mode register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Normal bus operation	3.3 V	3.3 V	3.3 V	5 V	enabled
Power loss	0 V	0 V	0 V	0 V	not applicable

Table 11. Operation truth table for clock off during suspend

ISP1582 operation	Power supply				Clock off during suspend
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Clock will wake up: After resume and After a bus reset	3.3 V	3.3 V	3.3 V	5 V	enabled
Power loss	0 V	0 V	0 V	0 V	not applicable

Table 12. Operation truth table for back voltage compliance

ISP1582 operation	Power supply				Bit SOFTCT in Mode register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
Back voltage is not measured in this mode	3.3 V	3.3 V	3.3 V	5 V	enabled
Power loss	0 V	0 V	0 V	0 V	not applicable

Table 13. Operation truth table for OTG

ISP1582 operation	Power supply				OTG register
	V_{CC}	$V_{CC(I/O)}$	RPU (3.3 V)	V_{BUS}	
SRP is not applicable	3.3 V	3.3 V	3.3 V	5 V	not applicable
Power loss	0 V	0 V	0 V	0 V	not applicable

8. Register description

Table 14. Register overview

Name	Destination	Address	Description	Size (bytes)	Reference
Initialization registers					
Address	device	00h	USB device address and enable	1	Section 8.2.1 on page 23
Mode	device	0Ch	power-down options, global interrupt enable, SoftConnect	2	Section 8.2.2 on page 24
Interrupt Configuration	device	10h	interrupt sources, trigger mode, output polarity	1	Section 8.2.3 on page 25
OTG	device	12h	OTG implementation	1	Section 8.2.4 on page 26
Interrupt Enable	device	14h	interrupt source enabling	4	Section 8.2.5 on page 28
Data flow registers					
Endpoint Index	endpoints	2Ch	endpoint selection, data flow direction	1	Section 8.3.1 on page 30
Control Function	endpoint	28h	endpoint buffer management	1	Section 8.3.2 on page 31
Data Port	endpoint	20h	data access to endpoint FIFO	2	Section 8.3.3 on page 32
Buffer Length	endpoint	1Ch	packet size counter	2	Section 8.3.4 on page 33
Buffer Status	endpoint	1Eh	buffer status for each endpoint	1	Section 8.3.5 on page 34
Endpoint MaxPacketSize	endpoint	04h	maximum packet size	2	Section 8.3.6 on page 35
Endpoint Type	endpoint	08h	selects endpoint type: isochronous, bulk or interrupt	2	Section 8.3.7 on page 36
DMA registers					
DMA Command	DMA controller	30h	controls all DMA transfers	1	Section 8.4.1 on page 38
DMA Transfer Counter	DMA controller	34h	sets byte count for DMA transfer	4	Section 8.4.2 on page 39
DMA Configuration	DMA controller	38h	sets GDMA configuration (counter enable, data strobing, bus width)	2	Section 8.4.3 on page 40
DMA Hardware	DMA controller	3Ch	endian type, signal polarity for DACK, DREQ, DIOW, DIOR, EOT	1	Section 8.4.4 on page 41
DMA Interrupt Reason	DMA controller	50h	shows reason (source) for DMA interrupt	2	Section 8.4.5 on page 42
DMA Interrupt Enable	DMA controller	54h	enables DMA interrupt sources	2	Section 8.4.6 on page 43
DMA Endpoint	DMA controller	58h	selects endpoint FIFO, data flow direction	1	Section 8.4.7 on page 43
DMA Burst Counter	DMA controller	64h	DMA burst counter	2	Section 8.4.8 on page 44

Table 14. Register overview *…continued*

Name	Destination	Address	Description	Size (bytes)	Reference
General registers					
Interrupt	device	18h	shows interrupt sources	4	Section 8.5.1 on page 45
Chip ID	device	70h	product ID code and hardware version	3	Section 8.5.2 on page 46
Frame Number	device	74h	last successfully received Start-Of-Frame: lower byte (byte 0) is accessed first	2	Section 8.5.3 on page 47
Scratch	device	78h	allows save or restore of firmware status during suspend	2	Section 8.5.4 on page 48
Unlock Device	device	7Ch	re-enables register write access after suspend	2	Section 8.5.5 on page 48
Test Mode	PHY	84h	direct setting of the DP and DM states, internal transceiver test (PHY)	1	Section 8.5.6 on page 49

8.1 Register access

The ISP1582 uses a 16-bit bus access. For single-byte registers, the upper byte (MSByte) must be ignored.

Endpoint specific registers are indexed using the Endpoint Index register. The target endpoint must be selected before accessing the following registers:

- Buffer length
- Buffer status
- Control function
- Data port
- Endpoint MaxPacketSize
- Endpoint type

Remark: Write zero to all reserved bits, unless otherwise specified.

8.2 Initialization registers

8.2.1 Address register (address: 00h)

This register sets the USB assigned address and enables the USB device. Table 15 shows the Address register bit allocation.

Bits DEVADDR will be cleared whenever a bus reset, a power-on reset or a soft reset occurs. Bit DEVEN will be cleared whenever a power-on reset or a soft reset occurs.

In response to the standard USB request SET_ADDRESS, the firmware must write the (enabled) device address to the Address register, followed by sending an empty packet to the host. The new device address is activated when the device receives an acknowledgment from the host for the empty packet token.

Table 15. Address register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DEVEN	DEVADDR[6:0]						
Reset	0	0	0	0	0	0	0	0
Bus reset	unchanged	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 16. Address register: bit description

Bit	Symbol	Description
7	DEVEN	**Device Enable**: Logic 1 enables the device. The device will not respond to the host, unless this bit is set.
6 to 0	DEVADDR [6:0]	**Device Address**: This field specifies the USB device address.

8.2.2 Mode register (address: 0Ch)

This register consists of 2 bytes (bit allocation: see Table 17).

The Mode register controls resume, suspend and wake-up behavior, interrupt activity, soft reset, clock signals and SoftConnect operation.

Table 17. Mode register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved						DMA CLKON	VBUSSTAT
Reset	-	-	-	-	-	-	0	-[1]
Bus reset	-	-	-	-	-	-	0	-[1]
Access	R	R	R	R	R	R	R/W	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CLKAON	SNDRSU	GOSUSP	SFRESET	GLINTENA	WKUPCS	PWRON	SOFTCT
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	unchanged	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] Value depends on the status of the V_{BUS} pin.

Table 18. Mode register: bit description

Bit	Symbol	Description
15 to 10	-	reserved
9	DMACLKON	**DMA Clock On**: **0 —** Power save mode; the DMA circuit will stop completely to save power. **1 —** Supply clock to the DMA circuit.
8	VBUSSTAT	**V_{BUS} Pin Status**: This bit reflects the V_{BUS} pin status.

Table 18. Mode register: bit description *…continued*

Bit	Symbol	Description
7	CLKAON	**Clock Always On**: Logic 1 indicates that internal clocks are always running when in the suspend state. Logic 0 switches off the internal oscillator and PLL when the device goes into suspend mode. The device will consume less power if this bit is set to logic 0. The clock is stopped about 2 ms after bit GOSUSP is set and then cleared.
6	SNDRSU	**Send Resume**: Writing logic 1, followed by logic 0 will generate an 10 ms upstream resume signal. **Remark:** The upstream resume signal is generated 5 ms after this bit is set to logic 0.
5	GOSUSP	**Go Suspend**: Writing logic 1, followed by logic 0 will activate suspend mode.
4	SFRESET	**Soft Reset**: Writing logic 1, followed by logic 0 will enable a software-initiated reset to the ISP1582. A soft reset is similar to a hardware-initiated reset (using pin RESET_N).
3	GLINTENA	**Global Interrupt Enable**: Logic 1 enables all interrupts. Individual interrupts can be masked by clearing the corresponding bits in the Interrupt Enable register. When this bit is not set, an unmasked interrupt will not generate an interrupt trigger on the interrupt pin. If global interrupt, however, is enabled while there is any pending unmasked interrupt, an interrupt signal will be immediately generated on the interrupt pin. (If the interrupt is set to pulse mode, the interrupt events that were generated before the global interrupt is enabled will not appear on the interrupt pin).
2	WKUPCS	**Wake up on Chip Select**: Logic 1 enables wake-up from suspend mode through a valid register read on the ISP1582. (A read will invoke the chip clock to restart. If you write to the register before the clock gets stable, it may cause malfunctioning).
1	PWRON	**Power On**: The SUSPEND pin output control. **0 —** The SUSPEND pin is HIGH when the ISP1582 is in the suspend state. Otherwise, the SUSPEND pin is LOW. **1 —** When the device is woken up from the suspend state, there will be a 1 ms active HIGH pulse on the SUSPEND pin. The SUSPEND pin will remain LOW in all other states.
0	SOFTCT	**SoftConnect**: Logic 1 enables the connection of the 1.5 kΩ pull-up resistor on pin RPU to the DP pin.

The status of the chip is shown in Table 19.

Table 19. Status of the chip

V_{BUS}	SoftConnect = on	SoftConnect = off
On	pull-up resistor on pin DP	pull-up resistor on pin DP is removed; suspend interrupt is generated after 3 ms of no bus activity
Off	pull-up resistor on pin DP is present; suspend interrupt is generated after 3 ms of no bus activity	pull-up resistor on pin DP is removed; suspend interrupt is generated after 3 ms of no bus activity

8.2.3 Interrupt Configuration register (address: 10h)

This 1-byte register determines the behavior and polarity of the INT output. The bit allocation is shown in Table 20. When the USB SIE receives or generates an ACK, NAK or NYET, it will generate interrupts, depending on three Debug mode fields.

CDBGMOD[1:0] — Interrupts for control endpoint 0

DDBGMODIN[1:0] — Interrupts for DATA IN endpoints 1 to 7

DDBGMODOUT[1:0] — Interrupts for DATA OUT endpoints 1 to 7

The Debug mode settings for CDBGMOD, DDBGMODIN and DDBGMODOUT allow you to individually configure when the ISP1582 sends an interrupt to the external microprocessor. Table 22 lists the available combinations.

Bit INTPOL controls the signal polarity of the INT output: active HIGH or LOW, rising or falling edge. For level-triggering, bit INTLVL must be made logic 0. By setting INTLVL to logic 1, an interrupt will generate a pulse of 60 ns (edge-triggering).

Table 20. Interrupt Configuration register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CDBGMOD[1:0]		DDBGMODIN[1:0]		DDBGMODOUT[1:0]		INTLVL	INTPOL
Reset	1	1	1	1	1	1	0	0
Bus reset	1	1	1	1	1	1	unchanged	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 21. Interrupt Configuration register: bit description

Bit	Symbol	Description
7 to 6	CDBGMOD[1:0]	**Control Endpoint 0 Debug Mode**: For values, see Table 22
5 to 4	DDBGMODIN[1:0]	**Data Debug Mode IN**: For values, see Table 22
3 to 2	DDBGMODOUT[1:0]	**Data Debug Mode OUT**: For values, see Table 22
1	INTLVL	**Interrupt Level**: Selects signaling mode on output INT (**0** = level; **1** = pulsed). In pulsed mode, an interrupt produces a 60 ns pulse.
0	INTPOL	**Interrupt Polarity**: Selects signal polarity on output INT (**0** = active LOW; **1** = active HIGH).

Table 22. Debug mode settings

Value	CDBGMOD	DDBGMODIN	DDBGMODOUT
00h	interrupt on all ACK and NAK	interrupt on all ACK and NAK	interrupt on all ACK, NYET and NAK
01h	interrupt on all ACK	interrupt on ACK	interrupt on ACK and NYET
1Xh	interrupt on all ACK and first NAK[1]	interrupt on all ACK and first NAK[1]	interrupt on all ACK, NYET and first NAK[1]

[1] First NAK: the first NAK on an IN or OUT token is generated after a set-up token and an ACK sequence.

8.2.4 OTG register (address: 12h)

The bit allocation of the OTG register is given in Table 23.

Table 23. OTG register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		DP	BSESSVALID	INITCOND	DISCV	VP	OTG
Reset	-	-	0	-	-	0	0	0
Bus reset	-	-	0	-	-	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

Table 24. OTG register: bit description

Bit	Symbol	Description[1][2][3]
7 to 6	-	reserved
5	DP	**Data Pulsing**: Used for data-line pulsing to toggle DP to generate the required data-line pulsing signal. The default value of this bit is logic 0. This bit must be cleared when data-line pulsing is completed.
4	BSESSVALID	**B-Session Valid**: The device can initiate another V_{BUS} discharge sequence after data-line pulsing and V_{BUS} pulsing, and before it clears this bit and detects a session valid. This bit is latched to logic 1 once V_{BUS} exceeds the B-device session valid threshold. Once set, it remains at logic 1. To clear this bit, write logic 1. (The ISP1582 continuously updates this bit to logic 1 when the B-session is valid. If the B-session is valid after it is cleared, it is set back to logic 1 by the ISP1582). **0 —** It implies that SRP has failed. To proceed to a normal operation, the device can restart SRP, clear bit OTG or proceed to an error handling process. **1 —** It implies that the B-session is valid. The device clears bit OTG, goes into normal operation mode, and sets bit SOFTCT (DP pull-up) in the Mode register. The OTG host has a maximum of 5 s before it responds to a session request. During this period, the ISP1582 may request to suspend. Therefore, the device firmware must wait for some time if it wishes to know the SRP result (success: if there is minimum response from the host within 5 s; failure; if there is no response from the host within 5 s).
3	INITCOND	**Initial Condition**: Write logic 1 to clear this bit. Wait for more than 2 ms and check the bit status. If it reads logic 0, it means that V_{BUS} remains lower than 0.8 V, and DP or DM are at SE0 during the elapsed time. The device can then start a B-device SRP. If it reads logic 1, it means that the initial condition of SRP is violated. So, the device must abort SRP. The bit is set to logic 1 by the ISP1582 when initial conditions are not met, and only writing logic 1 clears the bit. (If initial conditions are not met after this bit has been cleared, it will be set again). **Remark:** This implementation does not cover the case if an initial SRP condition is violated when this bit is read and data-line pulsing is started.
2	DISCV	**Discharge V_{BUS}**: Set to logic 1 to discharge V_{BUS}. The device discharges V_{BUS} before starting a new SRP. The discharge can take as long as 30 ms for V_{BUS} to be charged less than 0.8 V. This bit must be cleared (write logic 0) before starting a session end detection.
1	VP	**V_{BUS} Pulsing**: Used for V_{BUS} pulsing to toggle VP to generate the required V_{BUS} pulsing signal. This bit must be set for more than 16 ms and must be cleared before 26 ms.
0	OTG	**On-The-Go**: **1 —** Enables the OTG function. The V_{BUS} sensing functionality will be disabled. **0 —** Normal operation. All OTG control bits will be masked. Status bits are undefined.

[1] No interrupt is designed for OTG. The V_{BUS} interrupt, however, may assert as a side effect during the V_{BUS} pulsing (see note 2).

[2] When OTG is in progress, the V_{BUS} interrupt may be set because V_{BUS} is charged over the V_{BUS} sensing threshold or the OTG host has turned on the V_{BUS} supply to the device. Even if the V_{BUS} interrupt is found during SRP, the device must complete data-line pulsing and V_{BUS} pulsing before starting the B_SESSION_VALID detection.

[3] OTG implementation applies to the device with self-power capability. If the device works in sharing mode, it must provide a switch circuit to supply power to the ISP1582 core during SRP.

8.2.4.1 Session Request Protocol (SRP)

The ISP1582 can initiate an SRP. The B-device initiates SRP by data-line pulsing, followed by V_{BUS} pulsing. The A-device can detect either data-line pulsing or V_{BUS} pulsing.

The ISP1582 can initiate the B-device SRP by performing the following steps:

1. Set the OTG bit to start SRP.
2. Detect initial conditions by following the instructions given in bit INITCOND of the OTG register.
3. Start data-line pulsing: set bit DP of the OTG register to logic 1.
4. Wait for 5 ms to 10 ms.
5. Stop data-line pulsing: set bit DP of the OTG register to logic 0.
6. Start V_{BUS} pulsing: set bit VP of the OTG register to logic 1.
7. Wait for 10 ms to 20 ms.
8. Stop V_{BUS} pulsing: set bit VP of the OTG register to logic 0.
9. Discharge V_{BUS} for about 30 ms: optional by using bit DISCV of the OTG register.
10. Detect bit BSESSVALID of the OTG register for a successful SRP with bit OTG cleared.
11. Once bit BSESSVALID is detected, turn on the SOFTCT bit to start normal bus enumeration.

The B-device must complete both data-line pulsing and V_{BUS} pulsing within 100 ms.

Remark: When disabling OTG, data-line pulsing bit DP and V_{BUS} pulsing bit VP must be cleared by writing logic 0.

8.2.5 Interrupt Enable register (address: 14h)

This register enables or disables individual interrupt sources. The interrupt for each endpoint can individually be controlled using the associated bits IEPnRX or IEPnTX, here n represents the endpoint number. All interrupts can be globally disabled using bit GLINTENA in the Mode register (see Table 17).

An interrupt is generated when the USB SIE receives or generates an ACK or NAK on the USB bus. The interrupt generation depends on Debug mode settings of bit fields CDBGMOD[1:0], DDBGMODIN[1:0] and DDBGMODOUT[1:0] in the Interrupt Configuration register.

All data IN transactions use the Transmit buffers (TX), which are handled by bits DDBGMODIN[1:0]. All data OUT transactions go through the Receive buffers (RX), which are handled by bits DDBGMODOUT[1:0]. Transactions on control endpoint 0 (IN, OUT and SETUP) are handled by bits CDBGMOD[1:0].

Interrupts caused by events on the USB bus (SOF, suspend, resume, bus reset, set up and high-speed status) can also be individually controlled. A bus reset disables all enabled interrupts, except bit IEBRST (bus reset), which remains logic 1.

The Interrupt Enable register consists of 4 bytes. The bit allocation is given in Table 25.

Table 25. Interrupt Enable register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						IEP7TX	IEP7RX
Reset	-	-	-	-	-	-	0	0
Bus reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	IEP6TX	IEP6RX	IEP5TX	IEP5RX	IEP4TX	IEP4RX	IEP3TX	IEP3RX
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	IEP2TX	IEP2RX	IEP1TX	IEP1RX	IEP0TX	IEP0RX	reserved	IEP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IEVBUS	IEDMA	IEHS_STA	IERESM	IESUSP	IEPSOF	IESOF	IEBRST
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 26. Interrupt Enable register: bit description

Bit	Symbol	Description
31 to 26	-	reserved
25	IEP7TX	Logic 1 enables interrupt from the indicated endpoint.
24	IEP7RX	Logic 1 enables interrupt from the indicated endpoint.
23	IEP6TX	Logic 1 enables interrupt from the indicated endpoint.
22	IEP6RX	Logic 1 enables interrupt from the indicated endpoint.
21	IEP5TX	Logic 1 enables interrupt from the indicated endpoint.
20	IEP5RX	Logic 1 enables interrupt from the indicated endpoint.
19	IEP4TX	Logic 1 enables interrupt from the indicated endpoint.
18	IEP4RX	Logic 1 enables interrupt from the indicated endpoint.
17	IEP3TX	Logic 1 enables interrupt from the indicated endpoint.
16	IEP3RX	Logic 1 enables interrupt from the indicated endpoint.
15	IEP2TX	Logic 1 enables interrupt from the indicated endpoint.
14	IEP2RX	Logic 1 enables interrupt from the indicated endpoint.
13	IEP1TX	Logic 1 enables interrupt from the indicated endpoint.
12	IEP1RX	Logic 1 enables interrupt from the indicated endpoint.
11	IEP0TX	Logic 1 enables interrupt from the control IN endpoint 0.
10	IEP0RX	Logic 1 enables interrupt from the control OUT endpoint 0.
9	-	reserved
8	IEP0SETUP	Logic 1 enables interrupt for the set-up data received on endpoint 0.

Table 26. Interrupt Enable register: bit description *...continued*

Bit	Symbol	Description
7	IEVBUS	Logic 1 enables interrupt for V_{BUS} sensing.
6	IEDMA	Logic 1 enables interrupt on DMA Interrupt Reason register change detection.
5	IEHS_STA	Logic 1 enables interrupt on detection of a high-speed status change.
4	IERESM	Logic 1 enables interrupt on detection of a resume state.
3	IESUSP	Logic 1 enables interrupt on detection of a suspend state.
2	IEPSOF	Logic 1 enables interrupt on detection of a pseudo SOF.
1	IESOF	Logic 1 enables interrupt on detection of an SOF.
0	IEBRST	Logic 1 enables interrupt on detection of a bus reset.

8.3 Data flow registers

8.3.1 Endpoint Index register (address: 2Ch)

The Endpoint Index register selects a target endpoint for register access by the microcontroller. The register consists of 1 byte, and the bit allocation is shown in Table 27.

The following registers are indexed:

- Buffer length
- Buffer status
- Control function
- Data port
- Endpoint MaxPacketSize
- Endpoint type

For example, to access the OUT data buffer of endpoint 1 using the Data Port register, the Endpoint Index register has to be written first with 02h.

Remark: The Endpoint Index register and the DMA Endpoint register must not point to the same endpoint, irrespective of IN and OUT.

Remark: The delay time from the Write Endpoint Index register to the Read Data Port register must be at least 190 ns.

Remark: The delay time from the Write Endpoint Index register to the Write Data Port register must be at least 100 ns.

Table 27. Endpoint Index register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		EP0SETUP	ENDPIDX[3:0]				DIR
Reset	-	-	0	0	0	0	0	0
Bus reset	-	-	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 28. Endpoint Index register: bit description

Bit	Symbol	Description
7 to 6	-	reserved
5	EP0SETUP	**Endpoint 0 Setup**: Selects the SETUP buffer of endpoint 0. **0 —** Data buffer **1 —** SETUP buffer Must be logic 0 for access to endpoints other than set-up token buffer.
4 to 1	ENDPIDX[3:0]	**Endpoint Index**: Selects the target endpoint for register access of buffer length, buffer status, control function, data port, endpoint type and MaxPacketSize.
0	DIR	**Direction bit**: Sets the target endpoint as IN or OUT. **0 —** Target endpoint refers to OUT (RX) FIFO **1 —** Target endpoint refers to IN (TX) FIFO

Table 29. Addressing of endpoint buffers

Buffer name	EP0SETUP	ENDPIDX	DIR
SETUP	1	00h	0
Control OUT	0	00h	0
Control IN	0	00h	1
Data OUT	0	0Xh	0
Data IN	0	0Xh	1

8.3.2 Control Function register (address: 28h)

The Control Function register performs the buffer management on endpoints. It consists of 1 byte, and the bit configuration is given in Table 30. Register bits can stall, clear or validate any enabled data endpoint. Before accessing this register, the Endpoint Index register must first be written to specify the target endpoint.

Table 30. Control Function register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			CLBUF	VENDP	DSEN	STATUS	STALL
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	W	R/W	R/W

Table 31. Control Function register: bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	CLBUF	**Clear Buffer**: Logic 1 clears the TX or RX buffer of the indexed endpoint. The RX buffer is automatically cleared once the endpoint is completely read. This bit is set only when it is necessary to forcefully clear the buffer. For details, see Section 7.9. **Remark:** If using double buffer, to clear both the buffers issue the CLBUF command two times, that is, set and clear this bit two times.
3	VENDP	**Validate Endpoint**: Logic 1 validates data in the TX FIFO of an IN endpoint to send on the next IN token. In general, the endpoint is automatically validated when its FIFO byte count has reached endpoint MaxPacketSize. This bit is set only when it is necessary to validate the endpoint with the FIFO byte count, which is below endpoint MaxPacketSize. **Remark:** Use either bit VENDP or register Buffer Length to validate endpoint FIFO with FIFO bytes.
2	DSEN	**Data Stage Enable**: This bit controls the response of the ISP1582 to a control transfer. After the completion of the set-up stage, firmware must determine whether a data stage is required. For control OUT, firmware will set this bit and the ISP1582 goes into the data stage. Otherwise, the ISP1582 will NAK the data stage transfer. For control IN, firmware will set this bit before writing data to the TX FIFO and validate the endpoint. If no data stage is required, firmware can immediately set the STATUS bit after the set-up stage. **Remark:** The DSEN bit is cleared once the OUT token is acknowledged by the device and the IN token is acknowledged by the PC host. This bit cannot be read back and reading this bit will return logic 0.
1	STATUS	**Status Acknowledge**: Only applicable for control IN or OUT. This bit controls the generation of ACK or NAK during the status stage of a SETUP transfer. It is automatically cleared when the status stage is completed, or when a SETUP token is received. No interrupt signal will be generated. **0 —** Sends NAK **1 —** Sends an empty packet following the IN token (peripheral-to-host) or ACK following the OUT token (host-to-peripheral). **Remark:** The STATUS bit is cleared to zero once the zero-length packet is acknowledged by the device or the PC host. **Remark:** Data transfers preceding the status stage must first be fully completed before the STATUS bit can be set.
0	STALL	**Stall Endpoint**: Logic 1 stalls the indexed endpoint. This bit is not applicable for isochronous transfers. **Remark:** Stalling a data endpoint will confuse the Data Toggle bit about the stalled endpoint because the internal logic picks up from where it is stalled. Therefore, the Data Toggle bit must be reset by disabling and re-enabling the corresponding endpoint (by setting bit ENABLE to logic 0, followed by logic 1 in the Endpoint Type register) to reset the PID.

8.3.3 Data Port register (address: 20h)

This 2-byte register provides direct access for a microcontroller to the FIFO of the indexed endpoint. The bit allocation is shown in Table 32.

Peripheral-to-host (IN endpoint): After each write action, an internal counter is auto incremented by two to the next location in the TX FIFO. When all bytes are written (FIFO byte count = endpoint MaxPacketSize), the buffer is automatically validated. The data packet will then be sent on the next IN token. When it is necessary to validate the endpoint whose byte count is less than MaxPacketSize, it can be done using the Control Function register (bit VENDP) or the Buffer Length register.

Remark: The buffer can automatically be validated by using the Buffer Length register (see Table 34).

Host-to-peripheral (OUT endpoint): After each read action, an internal counter is auto decremented by two to the next location in the RX FIFO. When all bytes are read, buffer contents are automatically cleared. A new data packet can then be received on the next OUT token. Buffer contents can also be cleared using the Control Function register (bit CLBUF), when it is necessary to forcefully clear contents.

Remark: The delay time from the Write Endpoint Index register to the Read Data Port register must be at least 190 ns.

Remark: The delay time from the Write Endpoint Index register to the Write Data Port register must be at least 100 ns.

Table 32. Data Port register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	DATAPORT[15:8]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DATAPORT[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 33. Data Port register: bit description

Bit	Symbol	Description
15 to 8	DATAPORT[15:8]	data (upper byte)
7 to 0	DATAPORT[7:0]	data (lower byte)

8.3.4 Buffer Length register (address: 1Ch)

This register determines the current packet size (DATACOUNT) of the indexed endpoint FIFO. The bit allocation is given in Table 34.

The Buffer Length register is automatically loaded with the FIFO size, when the Endpoint MaxPacketSize register is written (see Table 38). A smaller value can be written when required. After a bus reset, the Buffer Length register is made zero.

IN endpoint: When data transfer is performed in multiples of MaxPacketSize, the Buffer Length register is not significant. This register is useful only when transferring data that is not a multiple of MaxPacketSize. The following two examples demonstrate the significance of the Buffer Length register.

Example 1: Consider that the transfer size is 512 bytes and the MaxPacketSize is programmed as 64 bytes, the Buffer Length register need not be filled. This is because the transfer size is a multiple of MaxPacketSize, and MaxPacketSize packets will be automatically validated because the last packet is also of MaxPacketSize.

Example 2: Consider that the transfer size is 510 bytes and the MaxPacketSize is programmed as 64 bytes, the Buffer Length register must be filled with 62 bytes just before the microprocessor writes the last packet of 62 bytes. This ensures that the last packet, which is a short packet of 62 bytes, is automatically validated.

Use bit VENDP in the Control register if you are not using the Buffer Length register.

This is applicable only to PIO mode access.

OUT endpoint: The DATACOUNT value is automatically initialized to the number of data bytes sent by the host on each ACK.

Remark: When using a 16-bit microprocessor bus, the last byte of an odd-sized packet is output as the lower byte (LSByte).

Remark: Buffer Length is valid only after an interrupt is generated for the OUT endpoint.

Table 34. Buffer Length register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	DATACOUNT[15:8]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DATACOUNT[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 35. Buffer Length register: bit description

Bit	Symbol	Description
15 to 0	DATACOUNT[15:0]	**Data Count**: Determines the current packet size of the indexed endpoint FIFO.

8.3.5 Buffer Status register (address: 1Eh)

This register is accessed using index. The endpoint index must first be set before accessing this register for the corresponding endpoint. It reflects the status of the double buffered endpoint FIFO.

Remark: This register is not applicable to the control endpoint.

Remark: For endpoint IN data transfer, firmware must ensure a 200 ns delay between writing of the data packet and reading the Buffer Status register. For endpoint OUT data transfer, firmware must also ensure a 200 ns delay between the reception of the endpoint interrupt and reading the Buffer Status register. For more information, refer to Ref. 3 "ISP1581/2/3 Frequently Asked Questions (AN10046)".

Table 36 shows the bit allocation of the Buffer Status register.

Table 36. Buffer Status register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						BUF1	BUF0
Reset	-	-	-	-	-	-	0	0
Bus reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R	R

Table 37. Buffer Status register: bit description

Bit	Symbol	Description
7 to 2	-	reserved
1 to 0	BUF[1:0]	**Buffer**: **00 —** The buffers are not filled. **01 —** One of the buffers is filled. **10 —** One of the buffers is filled. **11 —** Both the buffers are filled.

8.3.6 Endpoint MaxPacketSize register (address: 04h)

This register determines the maximum packet size for all endpoints, except control 0. The register contains 2 bytes, and the bit allocation is given in Table 38.

Each time the register is written, the Buffer Length register of the corresponding endpoint is re-initialized to the FFOSZ field value. Bits NTRANS control the number of transactions allowed in a single microframe (for high-speed isochronous and interrupt endpoints only).

Table 38. Endpoint MaxPacketSize register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			NTRANS[1:0]		FFOSZ[10:8]		
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FFOSZ[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 39. Endpoint MaxPacketSize register: bit description

Bit	Symbol	Description
15 to 13	-	reserved
12 to 11	NTRANS[1:0]	**Number of Transactions**: HS mode only. **00 —** 1 packet per microframe **01 —** 2 packets per microframe **10 —** 3 packets per microframe **11 —** reserved These bits are applicable only for isochronous or interrupt transactions.
10 to 0	FFOSZ[10:0]	**FIFO Size**: Sets the FIFO size, in bytes, for the indexed endpoint. Applies to both high-speed and full-speed operations.

The ISP1582 supports all the transfers given in Ref. 1 “Universal Serial Bus Specification Rev. 2.0”.

Each programmable FIFO can independently be configured using its Endpoint MaxPacketSize register (R/W: 04h), but the total physical size of all enabled endpoints (IN plus OUT) including set-up token buffer, control IN and control OUT, must not exceed 8192 bytes.

8.3.7 Endpoint Type register (address: 08h)

This register sets the endpoint type of the indexed endpoint: isochronous, bulk or interrupt. It also serves to enable the endpoint and configure it for double buffering. Automatic generation of an empty packet for a zero-length TX buffer can be disabled using bit NOEMPKT. The register contains 2 bytes, and the bit allocation is shown in Table 40.

Table 40. Endpoint Type register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	-	-	-	-	-	-	-	-
Bus reset	-	-	-	-	-	-	-	-
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			NOEMPKT	ENABLE	DBLBUF	ENDPTYP[1:0]	
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

Table 41. Endpoint Type register: bit description

Bit	Symbol	Description
15 to 5	-	reserved
4	NOEMPKT	**No Empty Packet**: Logic 0 causes the ISP1582 to return a null length packet for the IN token after the DMA IN transfer is complete. For the IN DMA transfer, which does not require a null length packet after DMA completion, set to logic 1 to disable the generation of the null length packet.
3	ENABLE	**Endpoint Enable**: Logic 1 enables the FIFO of the indexed endpoint. The memory size is allocated as specified in the Endpoint MaxPacketSize register. Logic 0 disables the FIFO. **Remark:** Stalling a data endpoint will confuse the Data Toggle bit on the stalled endpoint because the internal logic picks up from where it has stalled. Therefore, the Data Toggle bit must be reset by disabling and re-enabling the corresponding endpoint (by setting bit ENABLE to logic 0 or logic 1 in the Endpoint Type register) to reset the PID.
2	DBLBUF	**Double Buffering**: Logic 1 enables double buffering for the indexed endpoint. Logic 0 disables double buffering.
1 to 0	ENDPTYP[1:0]	**Endpoint Type**: These bits select the endpoint type as follows. **00 —** Not used **01 —** Isochronous **10 —** Bulk **11 —** Interrupt

8.4 DMA registers

The Generic DMA (GDMA) transfer can be done by writing the proper opcode in the DMA Command register. Control bits are given in Table 42.

GDMA read/write (opcode = 00h/01h) for GDMA mode: Depending on the MODE[1:0] bits set in the DMA configuration register, the DACK, DIOR or DIOW signal strobes data. These signals are driven by the external DMA controller.

GDMA mode can operate in either counter mode or EOT-only mode.

In counter mode, bit DIS_XFER_CNT in the DMA Configuration register must be set to logic 0. The DMA Transfer Counter register must be programmed before any DMA command is issued. The DMA transfer counter is set by writing from the LSByte to the MSByte (address: 34h to 37h). The DMA transfer count is internally updated only after the MSByte is written. Once the DMA transfer is started, the transfer counter starts decrementing and on reaching 0, bit DMA_XFER_OK is set and an interrupt is generated by the ISP1582. If the DMA master wishes to terminate the DMA transfer, it can issue an EOT signal to the ISP1582. This EOT signal overrides the transfer counter and can terminate the DMA transfer at any time.

In EOT-only mode, DIS_XFER_CNT must be set to logic 1. Although the DMA transfer counter can still be programmed, it will not have any effect on the DMA transfer. The DMA transfer will start once the DMA command is issued. Any of the following three ways will terminate this DMA transfer:

- Detecting an external EOT
- Detecting an internal EOT (short packet on an OUT token)

- Issuing a GDMA stop command

There are three interrupts programmable to differentiate the method of DMA termination: bits INT_EOT, EXT_EOT and DMA_XFER_OK in the DMA Interrupt Reason register. For details, see Table 54.

Table 42. Control bits for GDMA read/write (opcode = 00h/01h)

Control bits	Description	Reference
DMA Configuration register		
MODE[1:0]	determines the active read/write data strobe signals	Table 48
WIDTH	selects the DMA bus width: 8 or 16 bits	
DIS_XFER_CNT	disables the use of the DMA Transfer Counter	
DMA Hardware register		
EOT_POL	selects the polarity of the EOT signal	Table 50
ENDIAN[1:0]	determines whether the data is to be byte swapped or normal; applicable only in 16-bit mode	
ACK_POL, DREQ_POL, WRITE_POL, READ_POL	select polarity of DMA handshake signals	

Remark: The DMA bus defaults to 3-state, until a DMA command is executed. All the other control signals are not 3-stated.

8.4.1 DMA Command register (address: 30h)

The DMA Command register is a 1-byte register (for bit allocation, see Table 43) that initiates all DMA transfer activity on the DMA controller. The register is write-only: reading it will return FFh.

Remark: The DMA bus will be in 3-state, until a DMA command is executed.

Table 43. DMA Command register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DMA_CMD[7:0]							
Reset	1	1	1	1	1	1	1	1
Bus reset	1	1	1	1	1	1	1	1
Access	W	W	W	W	W	W	W	W

Table 44. DMA Command register: bit description

Bit	Symbol	Description
7 to 0	DMA_CMD[7:0]	DMA command code; see Table 45.

Table 45. DMA commands

Code	Name	Description
00h	GDMA Read	**Generic DMA IN token transfer**: Data is transferred from the external DMA bus to the internal buffer. Strobe: DIOW by external DMA controller.
01h	GDMA Write	**Generic DMA OUT token transfer**: Data is transferred from the internal buffer to the external DMA bus. Strobe: DIOR by external DMA controller.
02h to 0Dh	-	reserved
0Eh	Validate Buffer	**Validate Buffer (for debugging only)**: Request from the microcontroller to validate the endpoint buffer, following a DMA-to-USB data transfer.

Table 45. DMA commands *…continued*

Code	Name	Description
0Fh	Clear Buffer	**Clear Buffer**: Request from the microcontroller to clear the endpoint buffer, after a DMA-to-USB data transfer. Logic 1 clears the TX buffer of the indexed endpoint; the RX buffer is not affected. The TX buffer is automatically cleared once data is sent on the USB bus. This bit is set only when it is necessary to forcefully clear the buffer. **Remark:** If using double buffer, to clear both the buffers issue the Clear Buffer command two times, that is, set and clear this bit two times.
10h	-	reserved
11h	Reset DMA	**Reset DMA**: Initializes the DMA core to its power-on reset state. **Remark:** When the DMA core is reset during the Reset DMA command, the DREQ, DACK, DIOW and DIOR handshake pins will temporarily be asserted. This can confuse the external DMA controller. To prevent this, start the external DMA controller **only after** the DMA reset.
12h	-	reserved
13h	GDMA Stop	**GDMA stop**: This command stops the GDMA data transfer. Any data in the OUT endpoint that is not transferred by the DMA will remain in the buffer. The FIFO data for the IN endpoint will be written to the endpoint buffer. An interrupt bit will be set to indicate the completion of the DMA Stop command.
14h to FFh	-	reserved

8.4.2 DMA Transfer Counter register (address: 34h)

This 4-byte register sets up the total byte count for a DMA transfer (DMACR). It indicates the remaining number of bytes left for transfer. The bit allocation is given in Table 46.

For IN endpoint — Because there is a FIFO in the ISP1582 DMA controller, some data may remain in the FIFO during the DMA transfer. The maximum FIFO size is 8 bytes, and the maximum delay time for data to be shifted to endpoint buffer is 60 ns.

For OUT endpoint — Data will not be cleared from the endpoint buffer, until all the data is read from the DMA FIFO.

If the DMA counter is disabled in the DMA transfer, it will still decrement and rollover when it reaches zero.

Table 46. DMA Transfer Counter register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	DMACR4 = DMACR[31:24]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	DMACR3 = DMACR[23:16]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DMACR2 = DMACR[15:8]							

Bit	15	14	13	12	11	10	9	8
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DMACR1 = DMACR[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 47. DMA Transfer Counter register: bit description

Bit	Symbol	Description
31 to 24	DMACR4 = DMACR[31:24]	DMA transfer counter byte 4 (MSByte)
23 to 16	DMACR3 = DMACR[23:16]	DMA transfer counter byte 3
15 to 8	DMACR2 = DMACR[15:8]	DMA transfer counter byte 2
7 to 0	DMACR1 = DMACR[7:0]	DMA transfer counter byte 1 (LSByte)

8.4.3 DMA Configuration register (address: 38h)

This register defines the DMA configuration for GDMA mode. The DMA Configuration register consists of 2 bytes. The bit allocation is given in Table 48.

Table 48. DMA Configuration register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	-	-	-	-	-	-	-	-
Bus reset	-	-	-	-	-	-	-	-
Access	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DIS_XFER_CNT	reserved			MODE[1:0]		reserved	WIDTH
Reset	0	-	-	-	0	0	-	1
Bus reset	0	-	-	-	0	0	-	1
Access	R/W	-	-	-	R/W	R/W	-	R/W

Table 49. DMA Configuration register: bit description

Bit	Symbol	Description[1]
15 to 8	-	reserved
7	DIS_XFER_CNT	**Disable Transfer Count**: Logic 1 disables the DMA Transfer Counter (see Table 46).
6 to 4	-	reserved

Table 49. DMA Configuration register: bit description *…continued*

Bit	Symbol	Description[1]
3 to 2	MODE[1:0]	**Mode**: These bits affect GDMA handshake signals. **00 —** DIOW strobes data from the DMA bus into the ISP1582; DIOR puts data from the ISP1582 on the DMA bus. **01 —** DACK strobes data from the DMA bus into the ISP1582; DIOR puts data from the ISP1582 on the DMA bus. **10 —** DACK strobes data from the DMA bus into the ISP1582 and also puts data from the ISP1582 on the DMA bus. **11 —** reserved
1	-	reserved
0	WIDTH	**Width**: This bit selects the DMA bus width. **0 —** 8-bit data bus **1 —** 16-bit data bus

[1] The DREQ pin will be driven only after performing a write access to the DMA Configuration register (that is, after configuring the DMA Configuration register).

8.4.4 DMA Hardware register (address: 3Ch)

The DMA Hardware register consists of 1 byte. The bit allocation is shown in Table 50.

This register determines the polarity of bus control signals (EOT, DACK, DREQ, DIOR and DIOW). It also controls whether the upper and lower parts of the data bus are swapped (bits ENDIAN[1:0]).

Table 50. DMA Hardware register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ENDIAN[1:0]		EOT_POL	reserved	ACK_POL	DREQ_POL	WRITE_POL	READ_POL
Reset	0	0	0	-	0	1	0	0
Bus reset	0	0	0	-	0	1	0	0
Access	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Table 51. DMA Hardware register: bit description

Bit	Symbol	Description
7 to 6	ENDIAN[1:0]	**Endian**: These bits determine whether the data bus is swapped between the internal RAM and the DMA bus. **00 —** Normal data representation; 16-bit bus: MSByte on DATA[15:8], LSByte on DATA[7:0] **01 —** Swapped data representation; 16-bit bus: MSByte on DATA[7:0], LSByte on DATA[15:8] **10 —** reserved **11 —** reserved **Remark:** While operating with the 8-bit data bus, bits ENDIAN[1:0] must always be set to 00b.
5	EOT_POL	**EOT Polarity**: Selects the polarity of the End-Of-Transfer input. **0 —** EOT is active LOW **1 —** EOT is active HIGH
4	-	reserved; must be set to logic 0.

Table 51. DMA Hardware register: bit description *...continued*

Bit	Symbol	Description
3	ACK_POL	**Acknowledgment Polarity**: Selects the DMA acknowledgment polarity. **0 —** DACK is active LOW **1 —** DACK is active HIGH
2	DREQ_POL	**DREQ Polarity**: Selects the DMA request polarity. **0 —** DREQ is active LOW **1 —** DREQ is active HIGH
1	WRITE_POL	**Write Polarity**: Selects the DIOW strobe polarity. **0 —** DIOW is active LOW **1 —** DIOW is active HIGH
0	READ_POL	**Read Polarity**: Selects the DIOR strobe polarity. **0 —** DIOR is active LOW **1 —** DIOR is active HIGH

8.4.5 DMA Interrupt Reason register (address: 50h)

This 2-byte register shows the source(s) of DMA interrupt. Each bit is refreshed after a DMA command is executed. An interrupt source is cleared by writing logic 1 to the corresponding bit. On detecting the interrupt, the external microprocessor must read the DMA Interrupt Reason register and mask it with the corresponding bits in the DMA Interrupt Enable register to determine the source of the interrupt.

The bit allocation is given in Table 52.

Table 52. DMA Interrupt Reason register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	TEST3	reserved		GDMA_ STOP	EXT_EOT	INT_EOT	reserved	DMA_ XFER_OK
Reset	-	-	-	0	0	0	-	0
Bus reset	-	-	-	0	0	0	-	0
Access	R	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	-	-	-	-	-	-	-	-
Bus reset	-	-	-	-	-	-	-	-
Access	-	-	-	-	-	-	-	-

Table 53. DMA Interrupt Reason register: bit description

Bit	Symbol	Description
15	TEST3	This bit is set when the DMA transfer for a packet (OUT transfer) terminates before the whole packet has been transferred. This bit is a status bit, and the corresponding mask bit of this register is always logic 0. Writing any value other than logic 0 has no effect.
14 to 13	-	reserved
12	GDMA_STOP	**GDMA Stop**: When the GDMA_STOP command is issued to DMA Command registers, it means the DMA transfer has successfully terminated.

Table 53. DMA Interrupt Reason register: bit description *...continued*

Bit	Symbol	Description
11	EXT_EOT	**External EOT**: Logic 1 indicates that an external EOT is detected.
10	INT_EOT	**Internal EOT**: Logic 1 indicates that an internal EOT is detected; see Table 54.
9	-	reserved
8	DMA_XFER_OK	**DMA Transfer OK**: Logic 1 indicates that the DMA transfer is completed (DMA Transfer Counter has become zero).
7 to 0	-	reserved

Table 54. Internal EOT-functional relation with bit DMA_XFER_OK

INT_EOT	DMA_XFER_OK	Description
1	0	During the DMA transfer, there is a premature termination with short packet.
1	1	DMA transfer is completed with short packet and the DMA transfer counter has reached 0.
0	1	DMA transfer is completed without any short packet and the DMA transfer counter has reached 0.

8.4.6 DMA Interrupt Enable register (address: 54h)

This 2-byte register controls the interrupt generation of the source bits in the DMA Interrupt Reason register. The bit allocation is given in Table 55. The bit description is given in Table 53.

Logic 1 enables the interrupt generation. After a bus reset, interrupt generation is disabled, with the values turning to logic 0.

Table 55. DMA Interrupt Enable register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	TEST4	reserved		IE_GDMA_STOP	IE_EXT_EOT	IE_INT_EOT	reserved	IE_DMA_XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.4.7 DMA Endpoint register (address: 58h)

This 1-byte register selects a USB endpoint FIFO as a source or destination for DMA transfers. The bit allocation is given in Table 56.

Table 56. DMA Endpoint register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				EPIDX[2:0]			DMADIR
Reset	-	-	-	-	0	0	0	0
Bus reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

Table 57. DMA Endpoint register: bit description

Bit	Symbol	Description
7 to 4	-	reserved
3 to 1	EPIDX[2:0]	**Endpoint Index**: selects the indicated endpoint for DMA access
0	DMADIR	**DMA Direction** **0 —** Selects the RX/OUT FIFO for DMA read transfers **1 —** Selects the TX/IN FIFO for DMA write transfers

The DMA Endpoint register must not reference the endpoint that is indexed by the Endpoint Index register (2Ch) at any time. Doing so will result in data corruption. Therefore, if the DMA Endpoint register is unused, point it to an unused endpoint. If the DMA Endpoint register, however, is pointed to an active endpoint, the firmware must not reference the same endpoint on the Endpoint Index register.

8.4.8 DMA Burst Counter register (address: 64h)

Table 58 shows the bit allocation of the 2-byte register.

Table 58. DMA Burst Counter register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			BURSTCOUNTER[12:8]				
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BURSTCOUNTER[7:0]							
Reset	0	0	0	0	0	0	1	0
Bus reset	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 59. DMA Burst Counter register: bit description

Bit	Symbol	Description
15 to 13	-	reserved
12 to 0	BURST COUNTER [12:0]	**Burst Counter**: This register defines the burst length. The counter must be programmed to be a multiple of two in 16-bit mode. The value of the burst counter must be programmed so that the burst counter is a factor of the buffer size. It is used to determine the assertion and de-assertion of DREQ.

8.5 General registers

8.5.1 Interrupt register (address: 18h)

The Interrupt register consists of 4 bytes. The bit allocation is given in Table 60.

When a bit is set in the Interrupt register, it indicates that the hardware condition for an interrupt has occurred. When the Interrupt register content is nonzero, the INT output will be asserted corresponding to the Interrupt Enable register. On detecting the interrupt, the external microprocessor must read the Interrupt register and mask it with the corresponding bits in the Interrupt Enable register to determine the source of the interrupt.

Each endpoint buffer has a dedicated interrupt bit (EPnTX, EPnRX). In addition, various bus states can generate an interrupt: resume, suspend, pseudo SOF, SOF and bus reset. The DMA controller only has one interrupt bit: the source for a DMA interrupt is shown in the DMA Interrupt Reason register.

Each interrupt bit can individually be cleared by writing logic 1. The DMA Interrupt bit can be cleared by writing logic 1 to the related interrupt source bit in the DMA Interrupt Reason register, followed by writing logic 1 to the DMA bit of the Interrupt register.

Table 60. Interrupt register: bit allocation

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						EP7TX	EP7RX
Reset	-	-	-	-	-	-	0	0
Bus reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	EP6TX	EP6RX	EP5TX	EP5RX	EP4TX	EP4RX	EP3TX	EP3RX
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	EP2TX	EP2RX	EP1TX	EP1RX	EP0TX	EP0RX	reserved	EP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VBUS	DMA	HS_STAT	RESUME	SUSP	PSOF	SOF	BRESET
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 61. Interrupt register: bit description

Bit	Symbol	Description
31 to 26	-	reserved
25	EP7TX	logic 1 indicates the endpoint 7 TX buffer as interrupt source
24	EP7RX	logic 1 indicates the endpoint 7 RX buffer as interrupt source

Table 61. Interrupt register: bit description *…continued*

Bit	Symbol	Description
23	EP6TX	logic 1 indicates the endpoint 6 TX buffer as interrupt source
22	EP6RX	logic 1 indicates the endpoint 6 RX buffer as interrupt source
21	EP5TX	logic 1 indicates the endpoint 5 TX buffer as interrupt source
20	EP5RX	logic 1 indicates the endpoint 5 RX buffer as interrupt source
19	EP4TX	logic 1 indicates the endpoint 4 TX buffer as interrupt source
18	EP4RX	logic 1 indicates the endpoint 4 RX buffer as interrupt source
17	EP3TX	logic 1 indicates the endpoint 3 TX buffer as interrupt source
16	EP3RX	logic 1 indicates the endpoint 3 RX buffer as interrupt source.
15	EP2TX	logic 1 indicates the endpoint 2 TX buffer as interrupt source
14	EP2RX	logic 1 indicates the endpoint 2 RX buffer as interrupt source
13	EP1TX	logic 1 indicates the endpoint 1 TX buffer as interrupt source
12	EP1RX	logic 1 indicates the endpoint 1 RX buffer as interrupt source
11	EP0TX	logic 1 indicates the endpoint 0 data TX buffer as interrupt source
10	EP0RX	logic 1 indicates the endpoint 0 data RX buffer as interrupt source
9	-	reserved
8	EP0SETUP	logic 1 indicates that a SETUP token was received on endpoint 0
7	VBUS	logic 1 indicates a transition from LOW to HIGH transition on V_{BUS}
6	DMA	**DMA status**: Logic 1 indicates a change in the DMA Interrupt Reason register.
5	HS_STAT	**High speed status**: Logic 1 indicates a change from full-speed to high-speed mode (HS connection). This bit is not set, when the system goes into full-speed suspend.
4	RESUME	**Resume status**: Logic 1 indicates that a status change from suspend to resume (active) was detected.
3	SUSP	**Suspend status**: Logic 1 indicates that a status change from active to suspend was detected on the bus.
2	PSOF	**Pseudo SOF interrupt**: Logic 1 indicates that a pseudo SOF or µSOF was received. Pseudo SOF is an internally generated clock signal (full-speed: 1 ms period, high-speed: 125 µs period) is not synchronized to the USB bus SOF or µSOF.
1	SOF	**SOF interrupt**: Logic 1 indicates that a SOF or µSOF was received.
0	BRESET	**Bus reset**: Logic 1 indicates that a USB bus reset was detected. When bit OTG in the OTG register is set, BRESET will not be set, instead, this interrupt bit will report SE0 on DP and DM for 2 ms.

8.5.2 Chip ID register (address: 70h)

This read-only register contains the chip identification and hardware version numbers. The firmware must check this information to determine functions and features supported. The register contains 3 bytes, and the bit allocation is shown in Table 62.

Table 62. Chip ID register: bit allocation

Bit	23	22	21	20	19	18	17	16
Symbol	CHIPID[15:8]							
Reset	0	0	0	1	0	1	0	1
Bus reset	0	0	0	1	0	1	0	1
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CHIPID[7:0]							
Reset	1	0	0	0	0	0	1	0
Bus reset	1	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VERSION[7:0]							
Reset	0	0	1	1	0	0	0	0
Bus reset	0	0	1	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 63. Chip ID register: bit description

Bit	Symbol	Description
23 to 16	CHIPID[15:8]	**Chip ID**: lower byte (15h)
15 to 8	CHIPID[7:0]	**Chip ID**: upper byte (82h)
7 to 0	VERSION[7:0]	**Version**: version number (30h)

8.5.3 Frame Number register (address: 74h)

This read-only register contains the frame number of the last successfully received Start-Of-Frame (SOF). The register contains 2 bytes, and the bit allocation is given in Table 64. In case of 8-bit access, the register content is returned lower byte first.

Table 64. Frame Number register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved		MICROSOF[2:0]			SOFR[10:8]		
Reset	-	-	0	0	0	0	0	0
Bus reset	-	-	0	0	0	0	0	0
Access	-	-	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SOFR[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 65. Frame Number register: bit description

Bit	Symbol	Description
15 to 14	-	reserved
13 to 11	MICROSOF[2:0]	microframe number
10 to 0	SOFR[10:0]	frame number

8.5.4 Scratch register (address: 78h)

This 16-bit register can be used by the firmware to save and restore information. For example, the device status before it enters the suspend state. The bit allocation is given in Table 66.

Table 66. Scratch register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	SFIRH[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SFIRL[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 67. Scratch register: bit description

Bit	Symbol	Description
15 to 8	SFIRH[7:0]	Scratch firmware information register (higher byte)
7 to 0	SFIRL[7:0]	Scratch firmware information register (lower byte)

8.5.5 Unlock Device register (address: 7Ch)

To protect registers from getting corrupted when the ISP1582 goes into suspend, the write operation is disabled if bit PWRON in the Mode register is set to logic 0. In this case, when the chip resumes, the Unlock Device command must first be issued to this register before attempting to write to the rest of the registers. This is done by writing unlock code (AA37h) to this register. The bit allocation of the Unlock Device register is given in Table 68.

Table 68. Unlock Device register: bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ULCODE[15:8] = AAh							
Reset	not applicable							
Bus reset	not applicable							
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ULCODE[7:0] = 37h							

Bit	7	6	5	4	3	2	1	0
Reset	not applicable							
Bus reset	not applicable							
Access	W	W	W	W	W	W	W	W

Table 69. Unlock Device register: bit description

Bit	Symbol	Description
15 to 0	ULCODE[15:0]	**Unlock Code**: Writing data AA37h unlocks the internal registers and FIFOs for writing, following a resume.

When bit PWRON in the Mode register is logic 1, the chip is powered. In such a case, you do not need to issue the Unlock command because the microprocessor is powered and therefore, the RD_N, WR_N and CS_N signals maintain their states.

When bit PWRON is logic 0, the RD_N, WR_N and CS_N signals are floating because the microprocessor is not powered. To protect the ISP1582 registers from being corrupted during suspend, register write is locked when the chip goes into suspend. Therefore, you need to issue the Unlock command to unlock the ISP1582 registers.

8.5.6 Test Mode register (address: 84h)

This 1-byte register allows the firmware to set pins DP and DM to predetermined states for testing purposes. The bit allocation is given in Table 70.

Remark: Only one bit can be set to logic 1 at a time. This must be implemented for the Hi-Speed USB logo compliance testing. To exit test mode, power cycle is required.

Table 70. Test Mode register: bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FORCEHS	reserved		FORCEFS	PRBS	KSTATE	JSTATE	SE0_NAK
Reset	0	-	-	0	0	0	0	0
Bus reset	unchanged	-	-	unchanged	0	0	0	0
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

Table 71. Test Mode register: bit description

Bit	Symbol	Description
7	FORCEHS	**Force High-Speed**: Logic 1[1] forces the hardware to high-speed mode only and disables the chirp detection logic.
6 to 5	-	reserved
4	FORCEFS	**Force Full-Speed**: Logic 1[1] forces the physical layer to full-speed mode only and disables the chirp detection logic.
3	PRBS	**Predetermined Random Pattern**: Logic 1[2] sets pins DP and DM to toggle in a predetermined random pattern.
2	KSTATE	**K-State**: Logic logic 1[2] sets pins DP and DM to the K state.
1	JSTATE	**J-State**: Logic logic 1[2] sets pins DP and DM to the J state.
0	SE0_NAK	**SE0 NAK**: Logic logic 1[2] sets pins DP and DM to a high-speed quiescent state. The device only responds to a valid high-speed IN token with a NAK.

[1] Either FORCEHS or FORCEFS must be set at a time.

[2] Of the four bits (PRBS, KSTATE, JSTATE and SE0_NAK), only one bit must be set at a time.

9. Limiting values

Table 72. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{lu}	latch-up current	V_I < 0 V or V_I > V_{CC}		-	100	mA
V_{esd}	electrostatic discharge voltage	I_{LI} < 1 µA		–2000	+2000	V
T_{stg}	storage temperature			–40	+125	°C

[1] The maximum value for 5 V tolerant pins is 6 V.

10. Recommended operating conditions

Table 73. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	-	3.6	V
$V_{CC(I/O)}$	input/output supply voltage		V_{CC}	-	V_{CC}	V
V_I	input voltage	V_{CC} = 3.3 V	0	-	3.3	V
$V_{IA(I/O)}$	input voltage on analog I/O pins	on pins DP and DM	0	-	3.6	V
$V_{(pu)OD}$	open-drain pull-up voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+85	°C
T_j	junction temperature		–40	-	+125	°C

11. Static characteristics

Table 74. Static characteristics: supply pins

V_{CC} = 3.3 V ± 0.3 V; V_{GND} = 0 V; T_{amb} = –40 °C to +85 °C; typical values at T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage							
V_{CC}	supply voltage			3.0	3.3	3.6	V
I_{CC}	supply current	V_{CC} = 3.3 V					
		high-speed		-	45	60	mA
		full-speed		-	17	25	mA
$I_{CC(susp)}$	suspend supply current	V_{CC} = 3.3 V		-	160	-	µA
I/O pad supply voltage							
$V_{CC(I/O)}$	input/output supply voltage			V_{CC}	V_{CC}	V_{CC}	V
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$		[1]	-	3	-	mA
Regulated supply voltage							
$V_{CC(1V8)}$	supply voltage (1.8 V)	with voltage converter		1.65	1.8	1.95	V

[1] $I_{CC(I/O)}$ test condition: device set up under the test mode vector and I/O is subjected to external conditions.

Table 75. Static characteristics: digital pins

$V_{CC(I/O)} = V_{CC}$; $V_{GND} = 0$ V; $T_{amb} = -40$ °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC(I/O)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = rated drive	-	-	$0.15V_{CC(I/O)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = rated drive	$0.8V_{CC(I/O)}$	-	-	V
Leakage current						
I_{LI}	input leakage current	[1]	–5	-	+5	µA

[1] This value is applicable to transistor input only. The value will be different if internal pull-up or pull-down resistors are used.

Table 76. Static characteristics: OTG detection

$V_{CC(I/O)} = V_{CC}$; $V_{GND} = 0$ V; $T_{amb} = -40$ °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Charging and discharging resistor						
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	only when bit DISCV is set in the OTG register	680	800	1030	Ω
$R_{UP(DP)}$	pull-up resistance on pin DP	only when bit DP is set in the OTG register	300	550	780	Ω
Comparator levels						
V_{BVALID}	V_{BUS} valid detection		2.0	-	4.0	V
V_{SESEND}	V_{BUS} B-session end detection		0.2	-	0.8	V

Table 77. Static characteristics: analog I/O pins DP and DM

$V_{CC} = 3.3$ V ± 0.3 V; $V_{GND} = 0$ V; $T_{amb} = -40$ °C to +85 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{DI}	differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
V_{SE}	single-ended receiver threshold		0.8	-	2.0	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Schmitt-trigger inputs						
$V_{th(LH)}$	positive-going threshold voltage		1.4	-	1.9	V
$V_{th(HL)}$	negative-going threshold voltage		0.9	-	1.5	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to 3.6 V	-	-	0.4	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	2.8	-	3.6	V
Leakage current						
I_{LZ}	OFF-state leakage current	0 V < V_I < 3.3 V	–10	-	+10	µA

Table 77. Static characteristics: analog I/O pins DP and DM *...continued*

V_{CC} = 3.3 V ± 0.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	10	pF
Resistance						
Z_{DRV}	driver output impedance	steady-state drive	40.5	-	49.5	Ω
Z_{INP}	input impedance		10	-	-	MΩ

[1] Pin DP is the USB positive data pin, and pin DM is the USB negative data pin.

12. Dynamic characteristics

Table 78. Dynamic characteristics

V_{CC} = 3.3 V ± 0.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
$t_{W(RESET\_N)}$	external RESET_N pulse width	crystal oscillator running	500	-	-	µs
Crystal oscillator						
f_{XTAL1}	frequency on pin XTAL1		-	12	-	MHz
R_S	series resistance		-	-	100	Ω
C_L	load capacitance		-	18	-	pF
External clock input						
V_I	input voltage		1.65	1.8	1.95	V
t_J	external clock jitter		-	-	500	ps
δ	clock duty cycle		45	50	55	%
t_r	rise time		-	-	3	ns
t_f	fall time		-	-	3	ns

Table 79. Dynamic characteristics: analog I/O pins DP and DM

V_{CC} = 3.3 V ± 0.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; test circuit of Figure 22; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
Full-speed mode							
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$		4	-	20	ns
FRFM	differential rise time/fall time matching	t_{FR}/t_{FF}	[1]	90	-	111.11	%
V_{CRS}	output signal crossover voltage		[1][2]	1.3	-	2.0	V
High-speed mode							
t_{HSR}	rise time (10 % to 90 %)	with captive cable		500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	with captive cable		500	-	-	ps

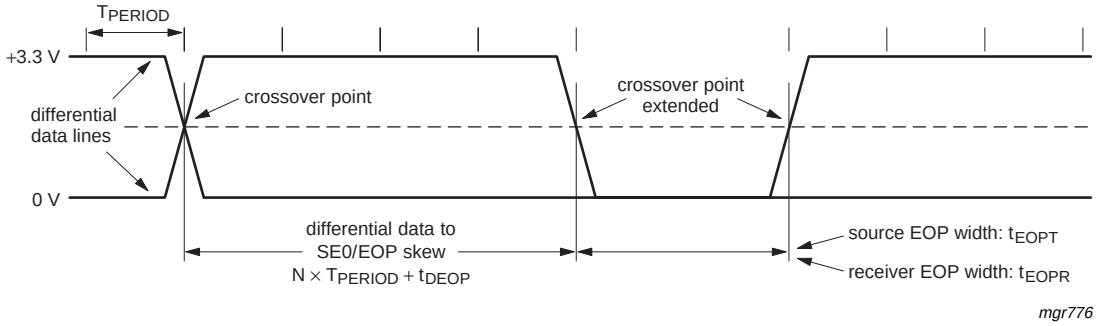
Table 79. Dynamic characteristics: analog I/O pins DP and DM *…continued*

V_{CC} = 3.3 V ± 0.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; test circuit of Figure 22; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Data source timing							
Full-speed mode							
t_{FEOPT}	source SE0 interval of EOP	see Figure 13	[2]	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 13	[2]	−2	-	+5	ns
Receiver timing							
Full-speed mode							
t_{JR1}	receiver jitter to next transition	see Figure 14	[2]	−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	see Figure 14	[2]	−9	-	+9	ns
t_{FEOPR}	receiver SE0 interval of EOP	accepted as EOP; see Figure 13	[2]	82	-	-	ns
t_{FST}	width of SE0 interval during differential transition	rejected as EOP; see Figure 15	[2]	-	-	14	ns

[1] Excluding the first transition from the idle state.

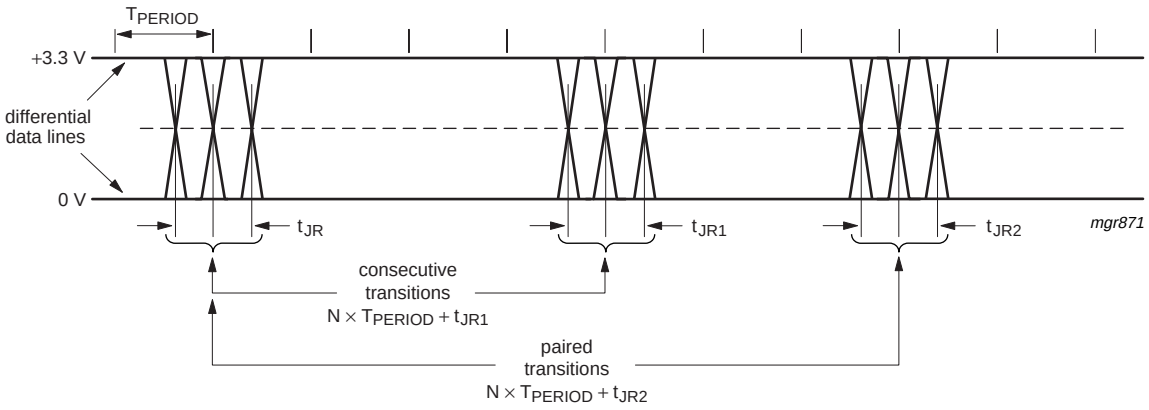
[2] Characterized only, not tested. Limits guaranteed by design.



T_{PERIOD} is the bit duration corresponding to the USB data rate.

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timing symbols have a prefix 'L'.

Fig 13. Source differential data-to-EOP transition skew and EOP width



T_{PERIOD} is the bit duration corresponding to the USB data rate.

Fig 14. Receiver differential data jitter

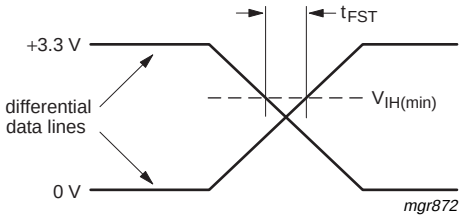


Fig 15. Receiver SE0 width tolerance

12.1 Register access timing

Table 80. Register access timing parameters: separate address and data buses

$V_{CC(I/O)}$ = V_{CC} = 3.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reading						
t_{RLRH}	RD_N LOW pulse width		> t_{RLDV}	-	-	ns
t_{AVRL}	address set-up time before RD_N LOW		0	-	-	ns
t_{RHAX}	address hold time after RD_N HIGH		0	-	-	ns
t_{RLDV}	RD_N LOW to data valid delay		-	-	26	ns
t_{RHDZ}	RD_N HIGH to data outputs 3-state delay		0	-	15	ns
t_{RHSH}	RD_N HIGH to CS_N HIGH delay		0	-	-	ns
t_{SLRL}	CS_N LOW to RD_N LOW delay		2	-	-	ns
Writing						
t_{WLWH}	WR_N LOW pulse width		15	-	-	ns
t_{AVWL}	address set-up time before WR_N LOW		0	-	-	ns
t_{WHAX}	address hold time after WR_N HIGH		0	-	-	ns
t_{DVWH}	data set-up time before WR_N HIGH		11	-	-	ns
t_{WHDZ}	data hold time after WR_N HIGH		5	-	-	ns
t_{WHSH}	WR_N HIGH to CS_N HIGH delay		0	-	-	ns

Table 80. Register access timing parameters: separate address and data buses *...continued*

$V_{CC(I/O)}$ = V_{CC} = 3.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SLWL}	CS_N LOW to WR_N LOW delay		2	-	-	ns
General						
$T_{cy(RW)}$	read or write cycle time		50	-	-	ns

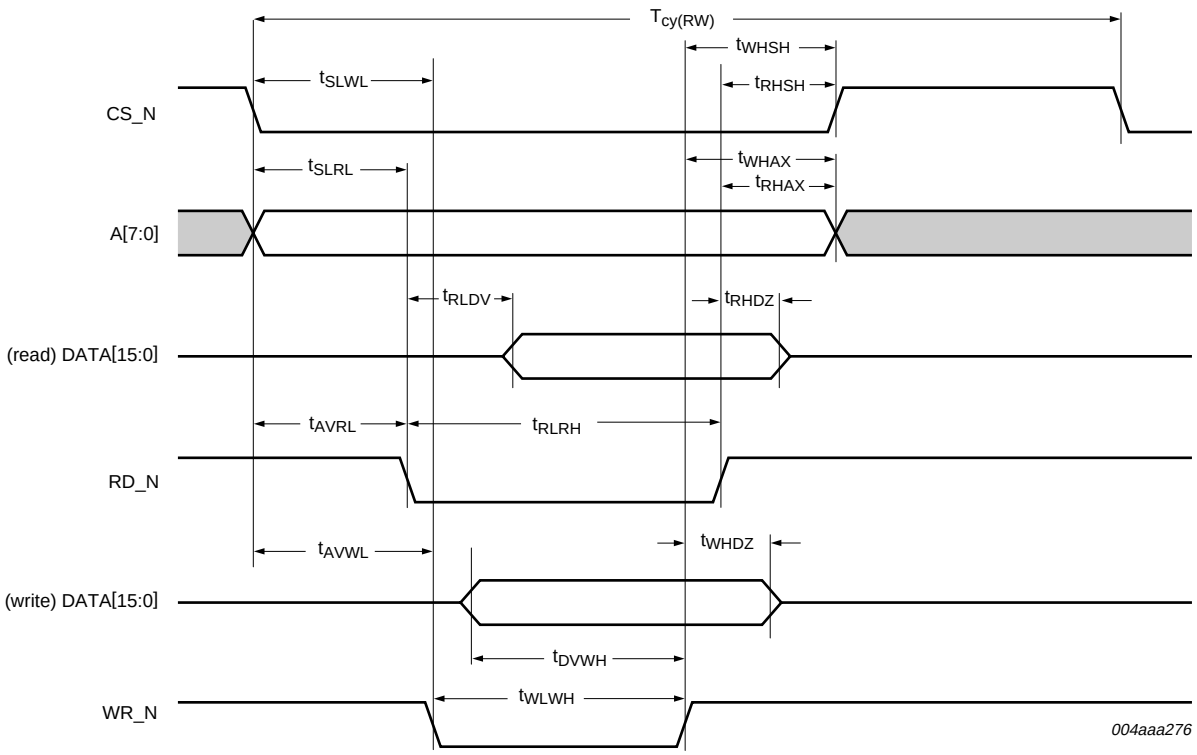


Fig 16. Register access timing: separate address and data buses

12.2 DMA timing

Table 81. GDMA mode timing parameters

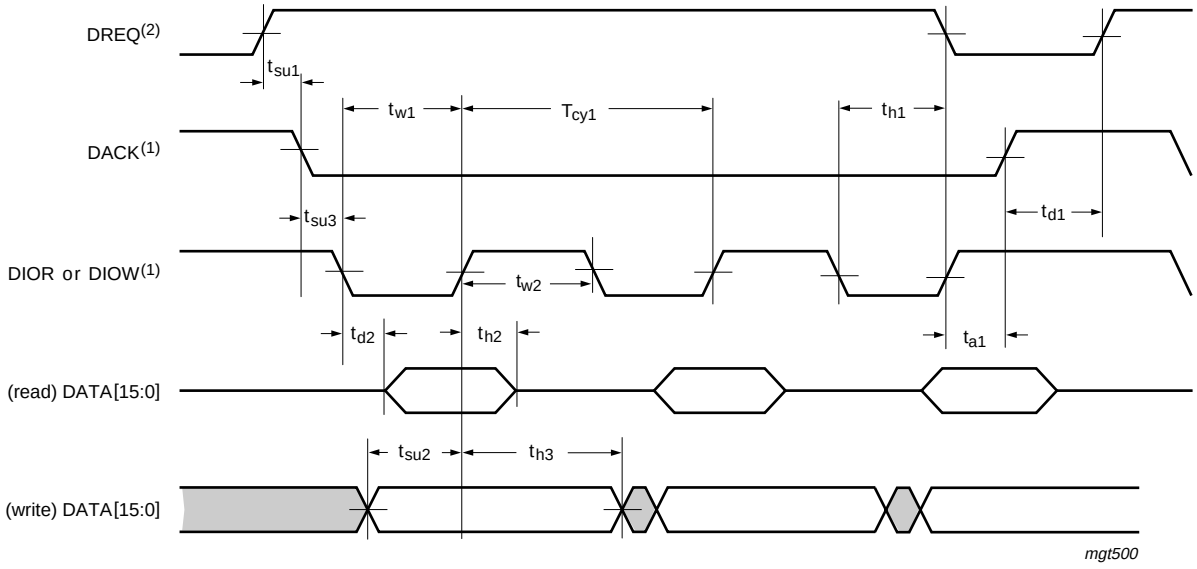
$V_{CC(I/O)}$ = V_{CC} = 3.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy1}	read or write cycle time		75	-	-	ns
t_{su1}	DREQ set-up time before first DACK on		10	-	-	ns
t_{d1}	DREQ on delay after last strobe off		33.33	-	-	ns
t_{h1}	DREQ hold time after last strobe on		0	-	53	ns
t_{w1}	DIOR or DIOW pulse width		39	-	600	ns
t_{w2}	DIOR or DIOW recovery time		36	-	-	ns
t_{d2}	read data valid delay after strobe on		-	-	20	ns
t_{h2}	read data hold time after strobe off		-	-	5	ns
t_{h3}	write data hold time after strobe off		1	-	-	ns

Table 81. GDMA mode timing parameters *…continued*

$V_{CC(I/O)}$ = V_{CC} = 3.3 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su2}	write data set-up time before strobe off		10	-	-	ns
t_{su3}	DACK set-up time before DIOR or DIOW assertion		0	-	-	ns
t_{a1}	DACK de-assertion after DIOR or DIOW de-assertion		0	-	30	ns



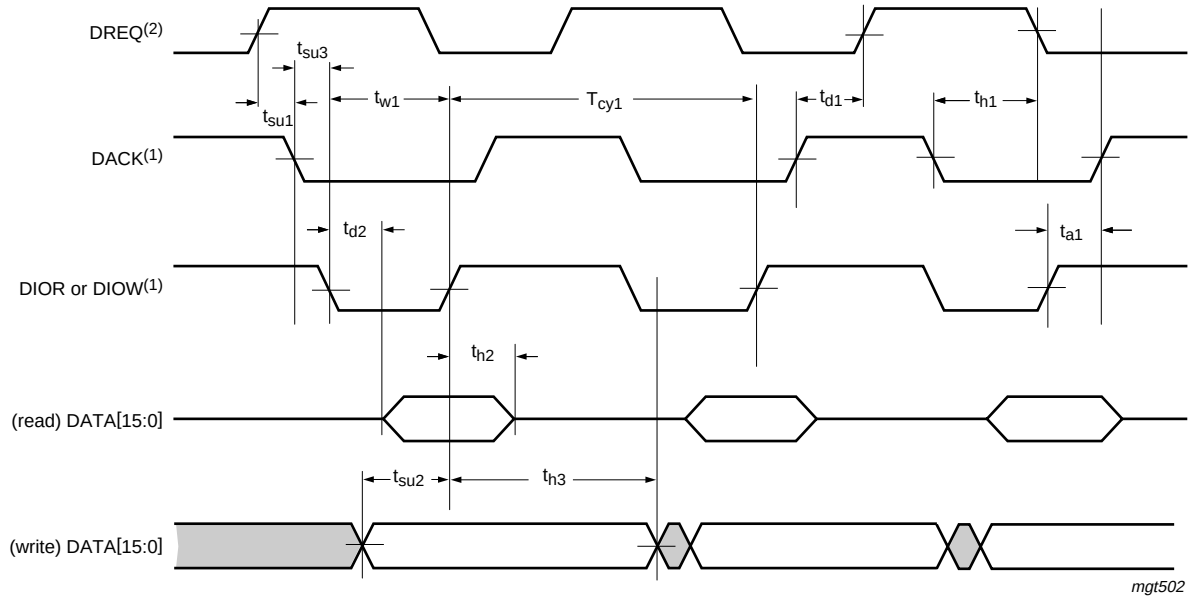
DREQ is continuously asserted, until the last transfer is done or the FIFO is full.

Data strobes: DIOR (read) and DIOW (write).

(1) Programmable polarity: shown as active LOW.

(2) Programmable polarity: shown as active HIGH.

Fig 17. GDMA mode timing (bits MODE[1:0] = 00)



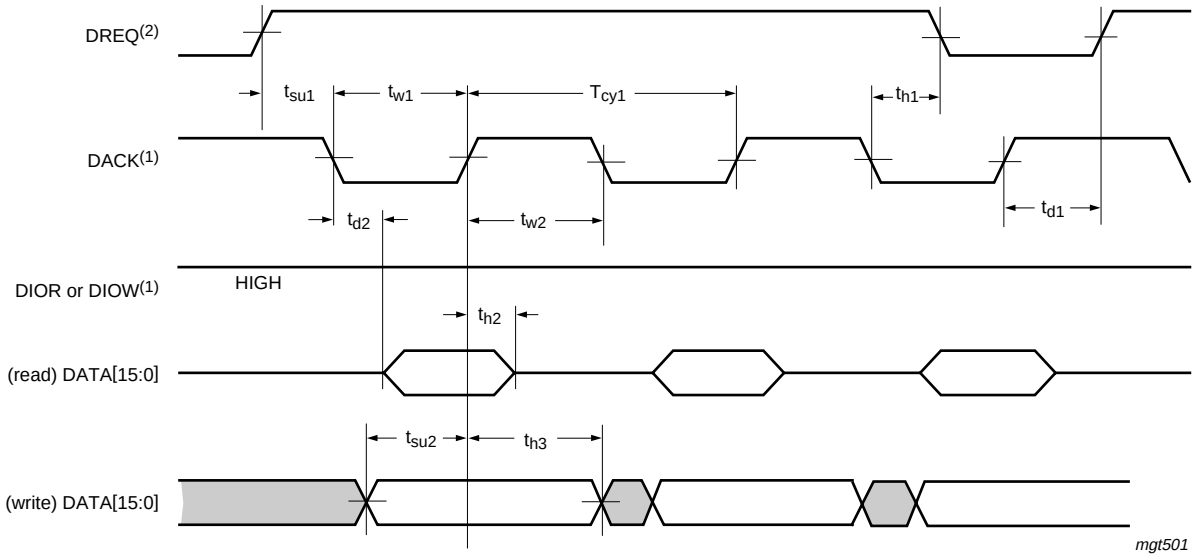
DREQ is asserted for every transfer.

Data strobes: DIOR (read) and DACK (write).

(1) Programmable polarity: shown as active LOW.

(2) Programmable polarity: shown as active HIGH.

Fig 18. GDMA mode timing (bits MODE[1:0] = 01)



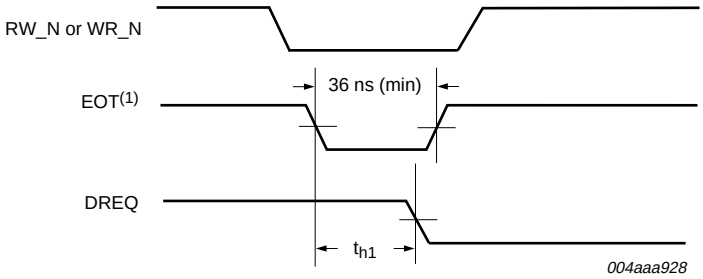
DREQ is continuously asserted, until the last transfer is done or the FIFO is full.

Data strobe: DACK (read/write).

(1) Programmable polarity: shown as active LOW.

(2) Programmable polarity: shown as active HIGH.

Fig 19. GDMA mode timing (bits MODE[1:0] = 10)



(1) Programmable polarity: shown as active LOW.

Remark: EOT must be valid for 36 ns (minimum) when RD_N or WR_N is active.

Fig 20. EOT timing in generic processor mode

13. Application information

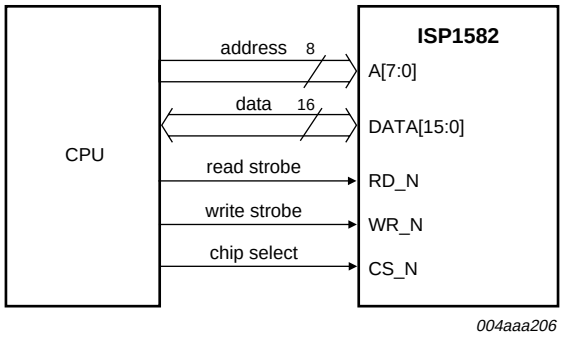
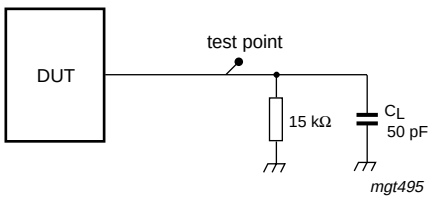


Fig 21. Typical interface connections for generic processor mode

14. Test information

The dynamic characteristics of the analog I/O ports DP and DM were determined using the circuit shown in Figure 22.

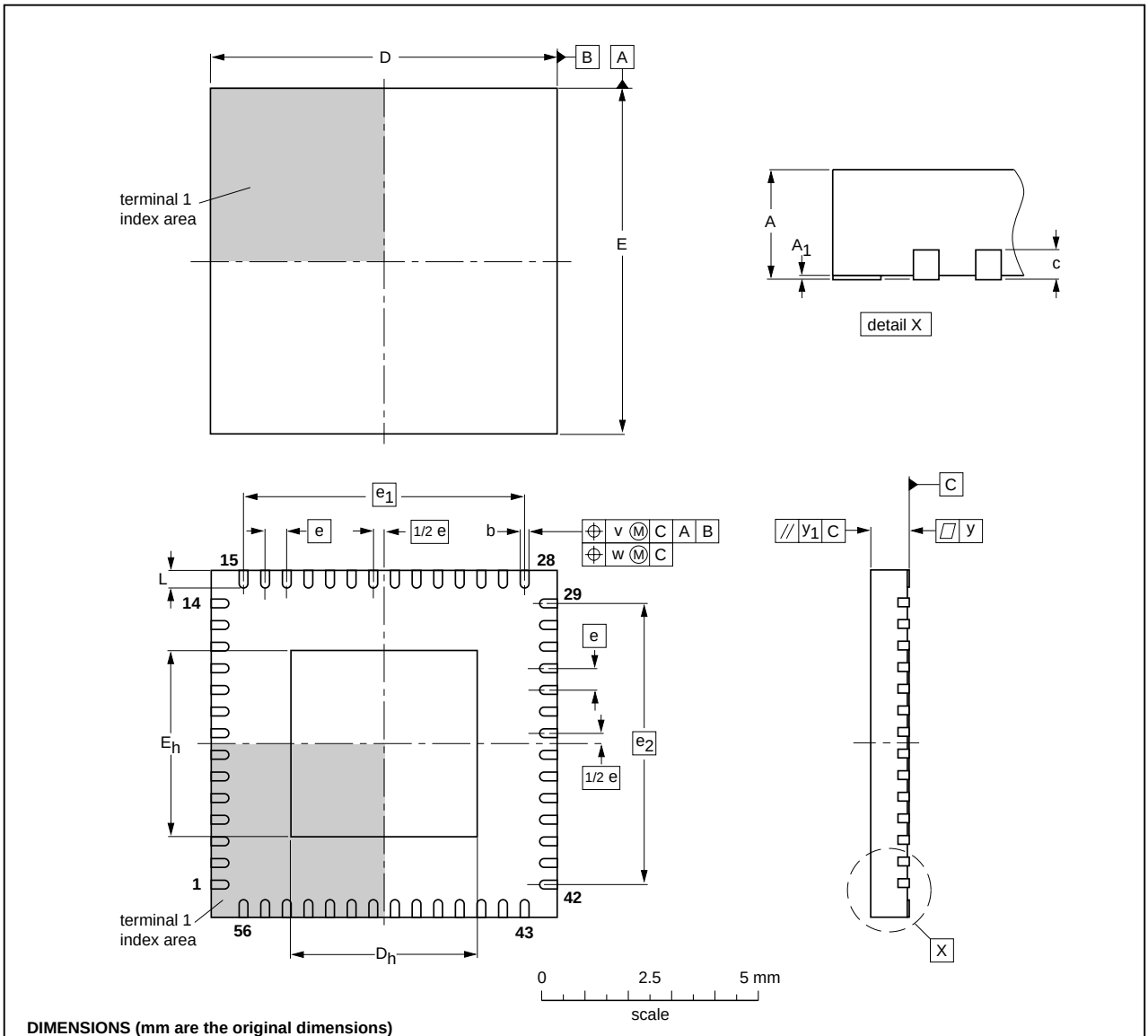


In full-speed mode, an internal 1.5 kΩ pull-up resistor is connected to pin DP.

Fig 22. Load impedance for pins DP and DM (full-speed mode)

15. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	8.1 7.9	4.45 4.15	8.1 7.9	4.45 4.15	0.5	6.5	6.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT684-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 23. Package outline SOT684-1 (HVQFN56)

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 82 and 83

Table 82. SnPb eutectic process (from J-STD-020C)

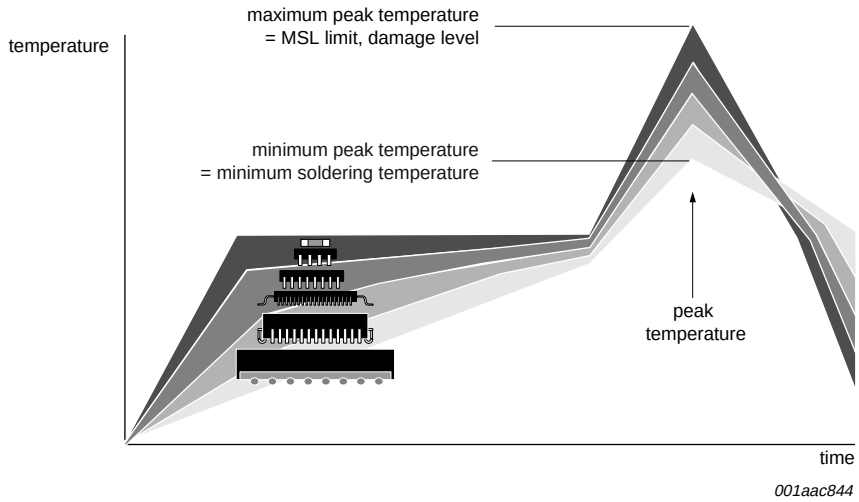
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 83. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 84. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
ASIC	Application-Specific Integrated Circuit
CRC	Cyclic Redundancy Code
DMA	Direct Memory Access
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
FS	Full-Speed
GDMA	Generic DMA
HS	High-Speed
MMU	Memory Management Unit
NRZI	Non-Return-to-Zero Inverted
OTG	On-The-Go
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PHY	Physical
PID	Packet IDentifier
PIE	Parallel Interface Engine
PIO	Parallel Input/Output
PLL	Phase-Locked Loop

Table 84. Abbreviations *...continued*

Acronym	Description
POR	Power-On Reset
SE0	Single-Ended zero
SIE	Serial Interface Engine
SRP	Session Request Protocol
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus

18. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB Specification Rev. 1.2

[3] ISP1581/2/3 Frequently Asked Questions (AN10046)

[4] ISP1582/83 and ISP1761 clearing an IN buffer (AN10045)

19. Revision history

Table 85. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1582_6	20070920	Product data sheet	-	ISP1582_5
Modifications:	• Updated Section 7.9 “Clear buffer”. • Added Section 7.10 “Reconfiguring endpoints”. • Table 5 “Power modes”: removed the last row. • Section 8.3.1 “Endpoint Index register (address: 2Ch)”: added two remarks. • Section 8.3.2 “Control Function register (address: 28h)”: updated the DSEN bit. • Section 8.3.3 “Data Port register (address: 20h)”: added two remarks. • Table 31 “Control Function register: bit description”: updated bit 4 description. • Table 33 “Data Port register: bit description”: updated the bit description. • Section 18 “References”: updated the list.			
ISP1582_5	20070201	Product data sheet	-	ISP1582-04
ISP1582-04 (9397 750 14033)	20050104	Product data	200412038	ISP1582-03
ISP1582-03 (9397 750 13699)	20040825	Preliminary data	-	ISP1582-02
ISP1582-02 (9397 750 12979)	20040629	Preliminary data	-	ISP1582-01
ISP1582-01 (9397 750 11496)	20040223	Preliminary data	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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